

SIT Change List

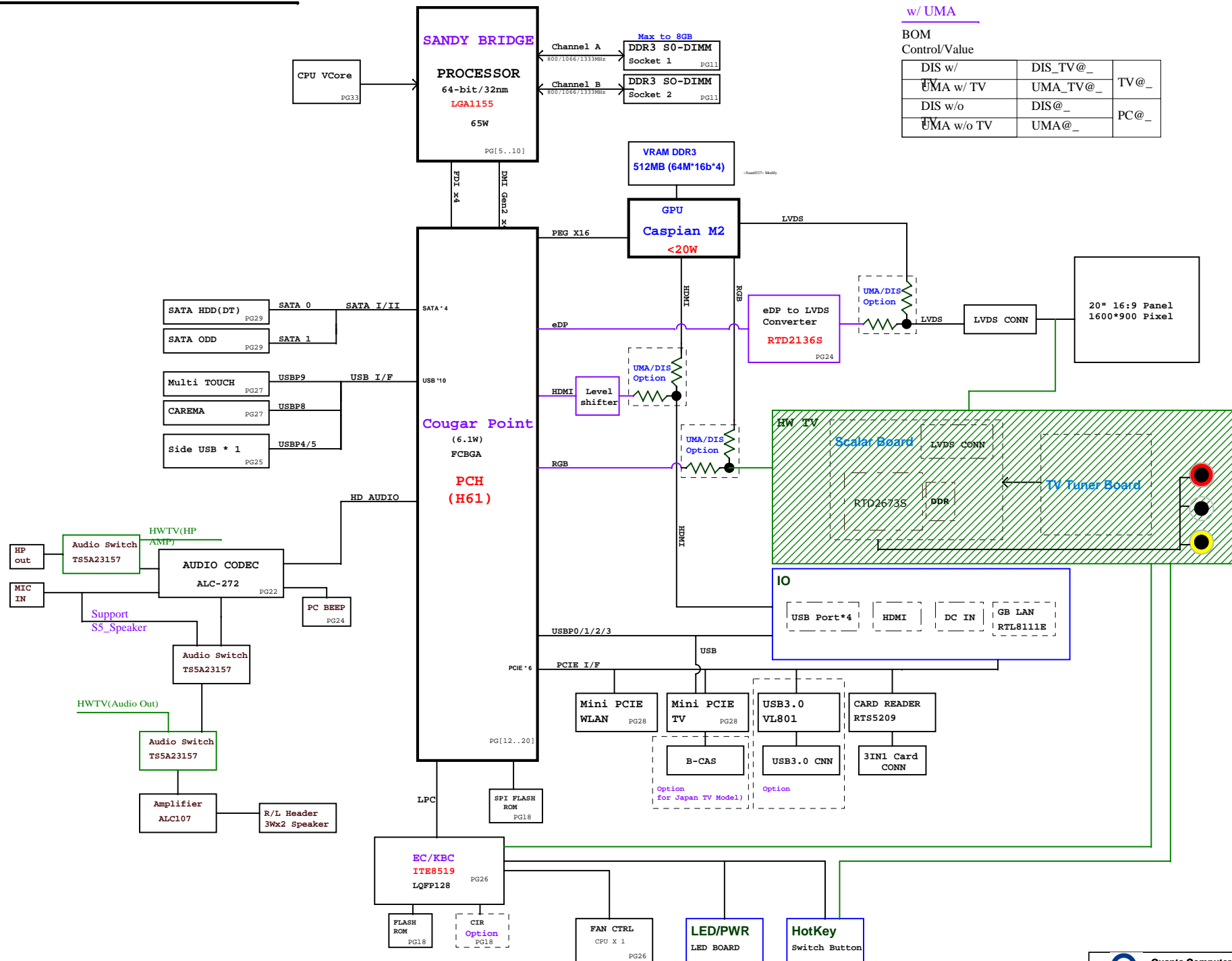
SIT-0427-01	15	change Q39 PIN Connect,Unmount R125	change Q39 PIN Connect for SATA Led always light issue ,Unmount R125
SIT-0420-01	37	change J98 PIN Define	meet new type FAN
SIT-0504-01	33	change Q40 PIN Connect	change Q40 PIN Connect for Wlan Led always light issue
SIT-0505-01	34/35	Mount R47/Unmount R341	for flash screen issue in discrete board
SIT-0510-01	36	ADD Q42/Mount R192 ,DEL R719	Support PCIe Wake up function
SIT-0510-01	16	Change USB30_SMI#_PCH from PCH GPIO24 to GPIO 13	GPIO 24 no USB30_SMI#_PCH Function
SIT-0511-01	30	add D21/D22	ADD D21/D22 FOR Current leakage
SIT-0511-01	33	add R724/R725/R726/Q45:Del C273/R361	Meet HDMI SPEC
SIT-0511-01	33	add R727 /Reserve Q44/Q43/R652	Meet VOL Command:reserve wlan wake up function
SIT-0511-01	7	un mount C4	H_PWRGD Rise time over SPEC
SIT-0512-01	33	DEL F2/F3/C262/C250/Q6/Q8/R365/R364/R354/R353	Cancel PCH Detect USB OC PIN/FUSE ADD Back IO BOARD
SIT-0512-01		del sense 电阻 PR111/PR112/PR133/PR156/PR170/PR171/PR198/PR222/PR241/PR181	C-Stage power sense 电阻 DEL
SIT-0512-01	42	PC82 Change to CC73301M200; Reserve PC254	Power concern
SIT-0512-01	16/12/15/21/20	ADD C273/C711/D25/D27/D28/C709, Reserve D24/D26	For ESD
SIT-0516-01	36	Q30 change to DTC144U	for current leakage issue under S4/S5
SIT-0516-01	34	D18 Connect to EC_PWRGD	
SIT-0516-01	29	Un-stuff AR76,AR77,AR78,AR79	vendor suggest
SIT-0516-01	29	AC47/AC52 Change to 100uP DIP cap	vendor suggest
SIT-0516-01	37/16	Add RN5/RN6/R353/R354	for LPC OVER/Under SHOOT
SIT-0516-01	29	ADD AR80	vendor suggest
SIT-0516-01	29	DEL AR70/AR75	vendor suggest
SIT-0516-01	29	AC48/AC50 Change to 0欧姆	vendor suggest
SIT-0516-01	29	del AR71/AR72/AR73/AR74/AR76/AR77/AR78/AR79	vendor suggest
SIT-0516-01	29	DEL AR64/AR65	vendor suggest
SIT-0516-01	29	AC43/AC44 Change to 0欧姆/0603	vendor suggest
SIT-0517-01	36	ADD D29	for KSD
SIT-0517-01	36	DEL R653/R654/R656/Q32	Cancel USB OC Detect function
SIT-0518-01	38/42	PR44 Unmount.Mount PR48,reserve PR170/PQ45	for ACPI SMDDR_VTERM fail
SIT-0518-01	36	Reserve C250/C262/FB6	for USB3.0 Device lost issue,change to 1.05V_S3
SIT-0518-01	41	ADD PQ46/PR181/PR171/PQ76/PR251	For 1.05V_S3 Discharge
SIT-0518-01	41	ADD PR133/PC255/PC253/PC260/PR131/PR132/PC259/PC257/PC258/PU15,reserve PC256	ADD 1.05V_S3 Power for USB3.0 Device lost issue
SIT-0518-01	38	Reserve PR284/PQ77	预留 12V_HDD Discharge
SIT-0518-01	16	reserve R361	STP_PCI_N Reserve PU/PD resistance for VERB Table control(TV/PC mode)
SIT-0519-01	20	ADD C712/D30/D32	For ESD
SIT-0519-01	36	U31 power PIN3/7/8 Change to USB30_+3.3VAUX	For Vendor suggest
SIT-0611-01		Stuff L1/L2/L11 Stuff L5/AC39/AC40/AC41/AC42 Stuff C113 Stuff C91/C284/C237/C206 Stuff R399/R400/R401/R402 Stuff R83/R109 Change to 22欧姆, atuf C573/C563/PC153/PC95/PC9 Reserve R206/R212	For EMI
SIT-0611-01	40	PR35 Change to 24.9K	Power concern
SIT-0611-01	39	PL10/PL13 Change to CV-2275M200	Power concern
SIT-0611-01	40	PC143 Change to 680p	Power concern
SIT-0611-01	33	Stuf C574/C581	For Wlan 1.5V Power
SIT-0611-01	39	PR227 Change to 150k/PR232 Change to 180k	Power concern
SIT-0611-01	44	PR137 Change to 3.57k	Power concern
SIT-0611-01	36	U10/U26 Change to RC101504200	For ESD
SIT-0611-01	40	Reseve PC60	Power concern

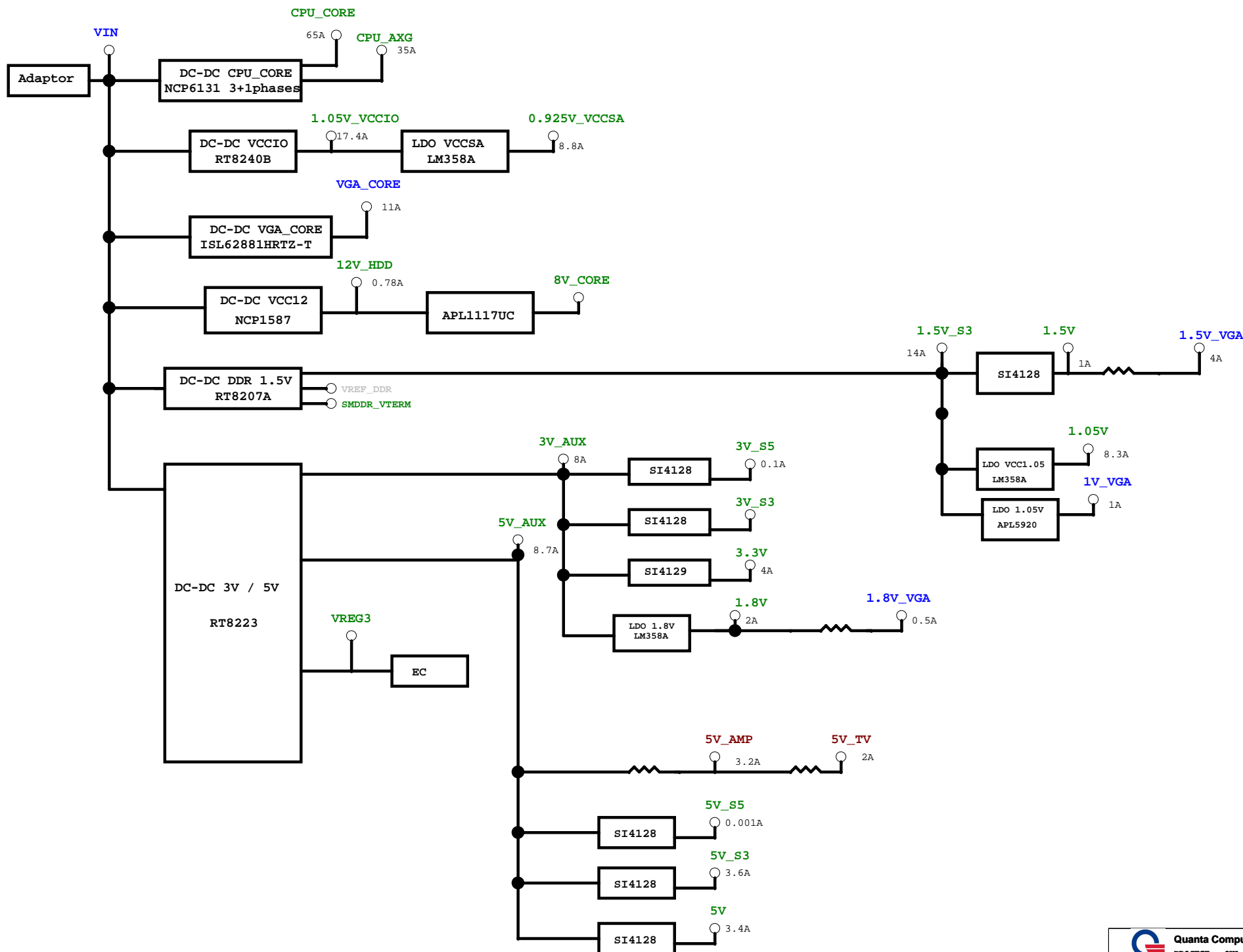
schematic Match BOM

After SIT Change List

SIT-0603-01	30	add F11/F12/F13 (DK300WPU000)	For safty
SIT-0603-01	41	Remove PQ64/PQ65	Power concern
SIT-0607-01	41	PQ37/PQ38 Change to BAW49260000	Power concern
SIT-0607-01	23	NO Stuff R198	for leakage current
SIT-0611-01	14	Del C709	For system hang up issue
SIT-0613-01	14/12	D24/D26 Reserve	
SIT-0613-01	30	JP61 footprint change to sata-ld1107f-s33t5-7p-r	follow SMT Requirement
SIT-0613-01	38	PR284 footprint from RCL206 to RC2512	Power concern
SIT-0704-01	33	Mount Q43/R652	Support Wlan wake up function

QUA Block Diagram





QUA Power sequence

Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	TV mode	Ctl Signal
VCCRTC	3.3V	ON	ON	ON	ON	ON		Battery IN
VIN	19V	ON	ON	ON	ON	OFF	ON	Adaptor IN
VREG3	3.3V	ON	ON	ON	ON	OFF	ON	VIN
5V_AUX	5V	ON	ON	OFF	OFF	OFF	ON	3V5V_ON
3V_AUX	3.3V	ON	ON	OFF	OFF	OFF	ON	3V5V_ON
5V_AMP	5V	ON	ON	OFF	OFF	OFF	ON	5V_AUX
5V_TV	5V	ON	ON	OFF	OFF	OFF	ON	5V_AMP
5V_S5	5V	ON	ON	OFF	OFF	OFF	OFF	S5_ON
3V_S5	3.3V	ON	ON	OFF	OFF	OFF	OFF	S5_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	OFF	S3_ON
3V_S3	3.3V	ON	ON	OFF	OFF	OFF	OFF	S3_ON
12V_HDD	12V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON1
5V	5V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON1
3.3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON1
1.8V	1.8V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON2
1.5V	1.5V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON2
1.05V	1.05V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON2
1.05V_VCCIO	1.05V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON2
SMDDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON2
1V_VGA	1V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON2
8V_CORE	8V	ON	OFF	OFF	OFF	OFF	OFF	12V_HDD
VGA_CORE	0.8V-1.15V	ON	OFF	OFF	OFF	OFF	OFF	VGA_ON
1.8V_VGA	1.8V	ON	OFF	OFF	OFF	OFF	OFF	1.8V
1.5V_VGA	1.5V	ON	OFF	OFF	OFF	OFF	OFF	1.5V
0.95V_VCCSA	0.95V	ON	OFF	OFF	OFF	OFF	OFF	VR_PVCCUSA_SEL
CPU_CORE	by SVID	ON	OFF	OFF	OFF	OFF	OFF	VR_ON
CPU_AXG	by SVID	ON	OFF	OFF	OFF	OFF	OFF	VR_ON



Note: Red Color is Gen2 spec.

Note: R0 is 0 ohm optional resistor

Note: Rs is series resistor

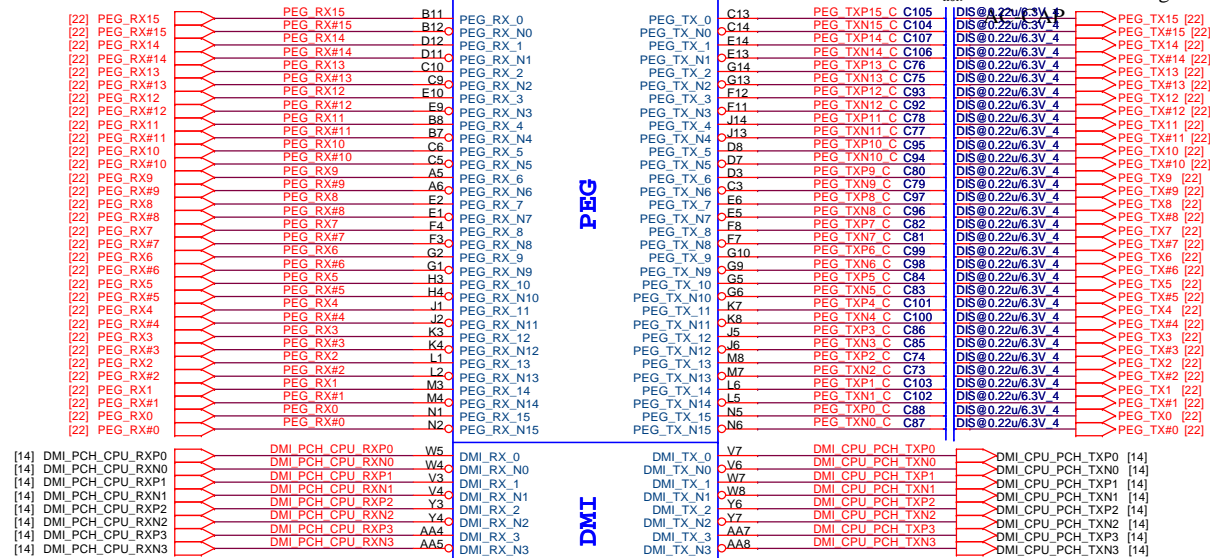
BTM: Buffer Through Mode
Need CK505 to provide 4 clock to PCH

FCIM: Full Clock Intergration Mode
Remove CK505

XU1C

<SEAN0331> change

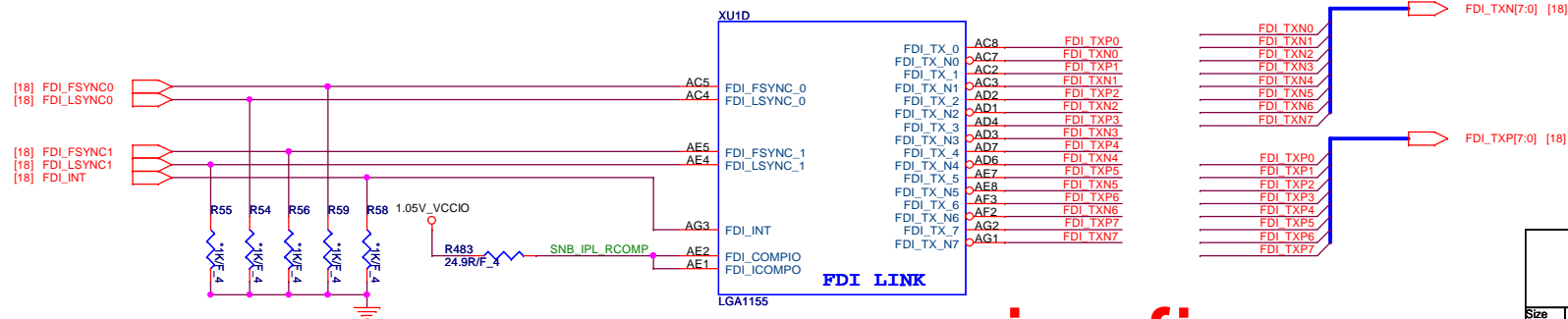
X5R

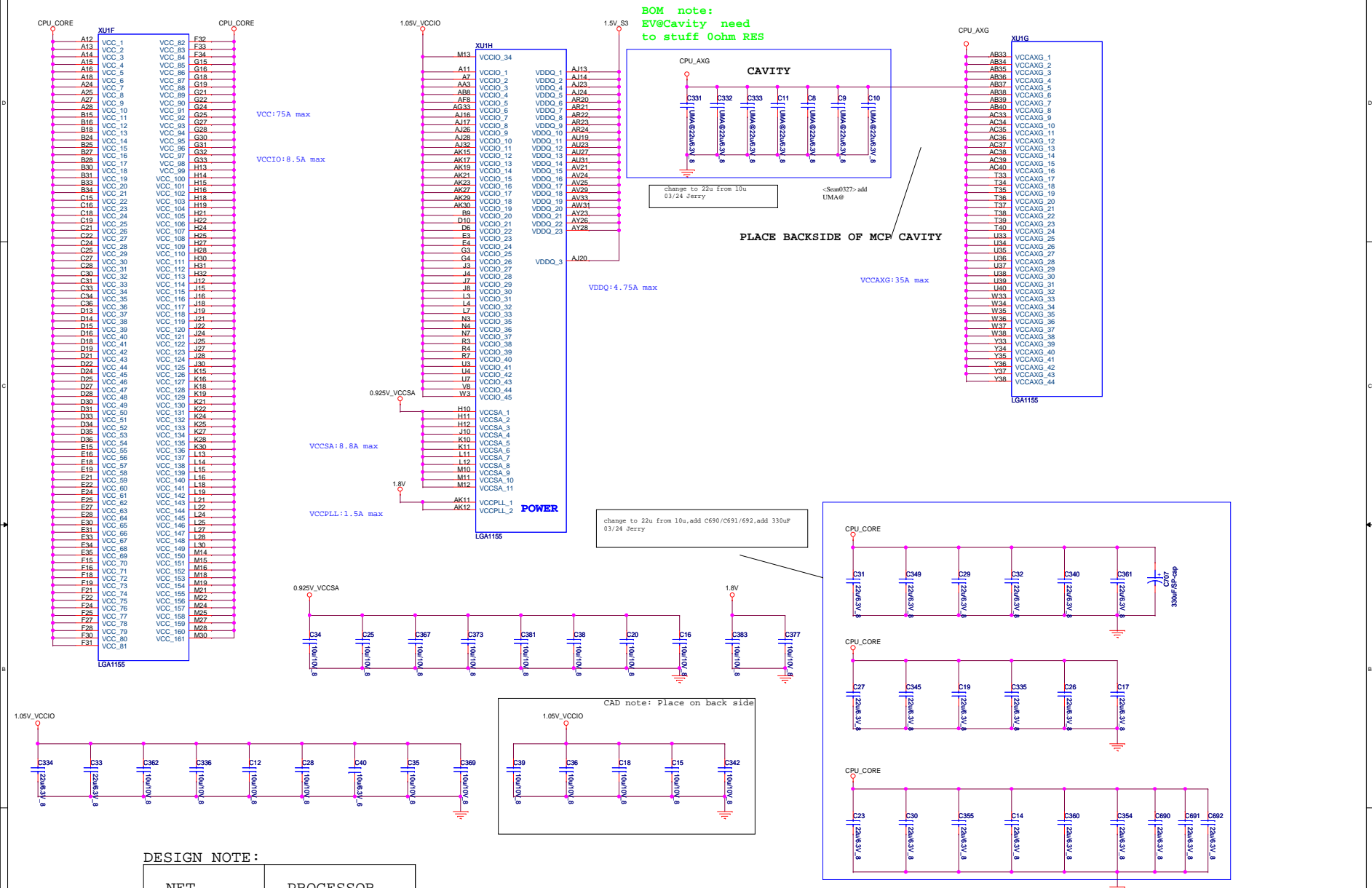


CAD NOTE:
PIN B5 ROUTING TO RESISTOR NEED TO BE 5 MILS
PIN C4 AND B4 ROUTING TO RESISTOR NEED TO BE 4 MILS
THERE ARE SPACING RULES ALSO - CHECK RULES DOCUMENT

FDI DISABLE GUIDELINES (FROM PDG)

FDI SIGNAL	RECOMMENDATION
FDI_TX[7:0]	FLOAT
FDI_TX_N[7:0]	FLOAT
FDI_FSYNC	1K RESISTOR TO VCC_FDI OR VSS
FDI_LSYNC	1K RESISTOR TO VCC_FDI OR VSS
FDI_INT	1K RESISTOR TO VCC_FDI OR VSS

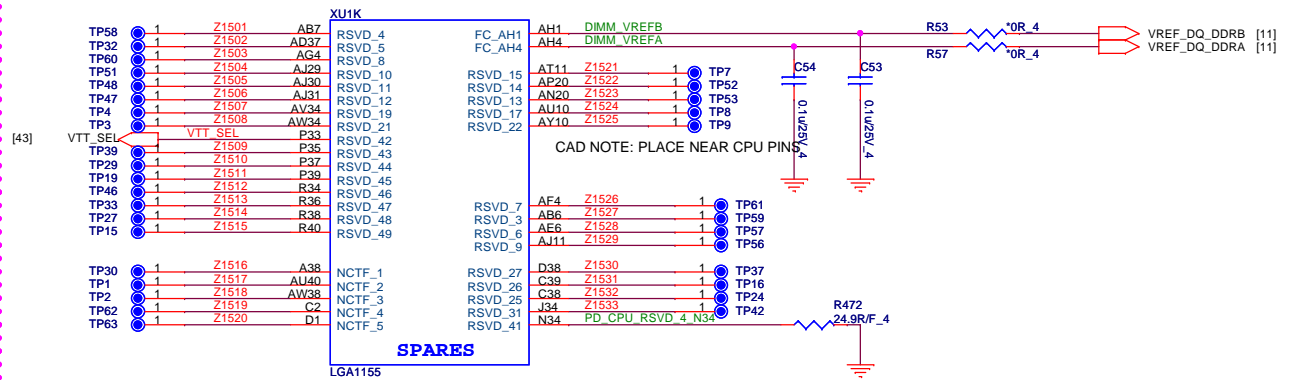


2011C: 65W TDP desktop
and server/workstation SKUs

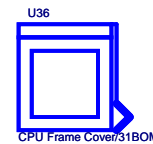
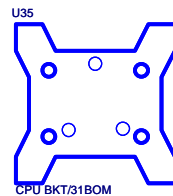
DESIGN NOTE:	
NET	PROCESSOR
CPU_CORE	SVID
CPU_AXG	SVID
1.05V_VCCIO	1.05V
0.925V_VCCSA	0.925V
1.5V_S3	1.5V
1.8V	1.8V

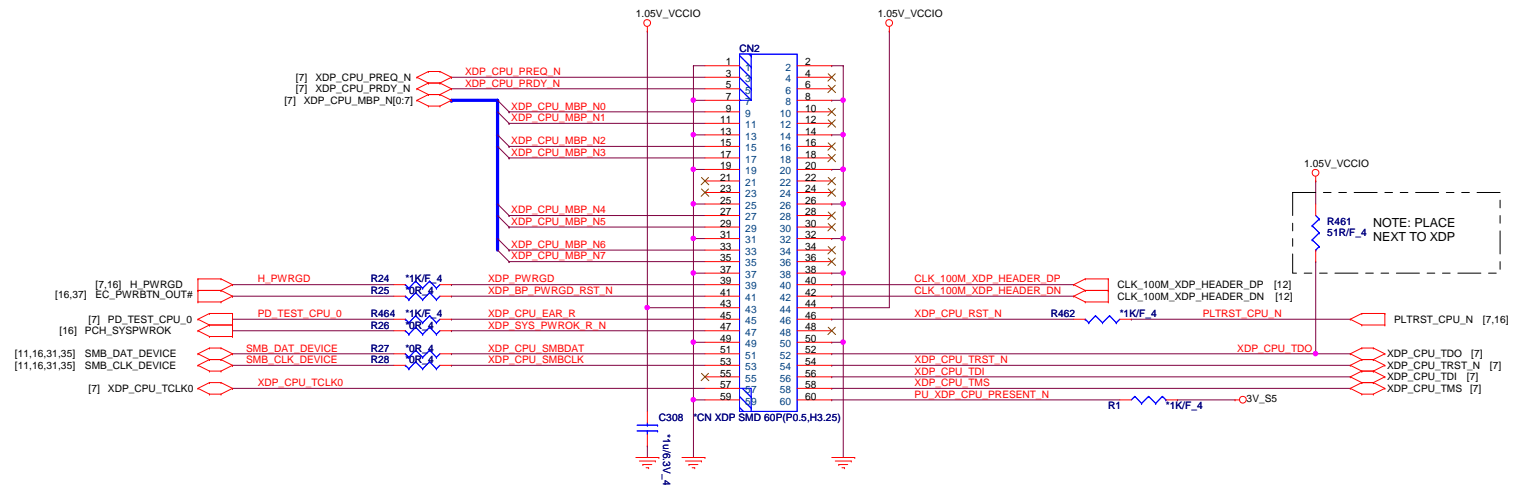
XU11			XU1J		
A17	VSS_1	VSS_91	AV11	VSS_181	VSS_271
A23	VSS_2	AM3	AV14	VSS_182	H1
A26	VSS_3	AM30	AV17	VSS_183	H17
A29	VSS_4	AM36	AV3	VSS_184	H2
A35	VSS_5	VSS_95	AV35	VSS_185	H20
AA33	VSS_6	VSS_96	AV38	VSS_186	H23
AA34	VSS_7	VSS_97	AV6	VSS_187	H26
AA35	VSS_8	VSS_98	AW10	VSS_188	H29
AA36	VSS_9	VSS_99	AW11	VSS_189	H33
AA37	VSS_10	AM5	AW14	VSS_190	H35
AA38	VSS_11	AN10	AW16	VSS_191	H37
AA6	VSS_12	VSS_102	AW36	VSS_192	H39
AB5	VSS_13	VSS_103	AW6	VSS_193	H6
AC1	VSS_14	AN14	AY11	VSS_194	H9
AC6	VSS_15	AN19	AY14	VSS_195	J11
AD33	VSS_16	VSS_105	AY18	VSS_196	J17
AD36	VSS_17	VSS_106	AY35	VSS_197	J20
AD38	VSS_18	VSS_107	AY4	VSS_198	J23
AD39	VSS_19	VSS_108	AY6	VSS_199	J26
AD40	VSS_20	VSS_109	AY8	VSS_200	J29
AD5	VSS_21	VSS_110	AN32	VSS_201	J32
AD8	VSS_22	VSS_111	AN33	VSS_202	K1
AE3	VSS_23	VSS_112	AN34	VSS_203	K12
AE33	VSS_24	VSS_113	AN35	VSS_204	K13
AE36	VSS_25	VSS_114	AN36	VSS_205	K14
AF1	VSS_26	VSS_115	AN6	VSS_206	K17
AF34	VSS_27	VSS_116	AN6	VSS_207	K2
AF36	VSS_28	VSS_117	AN7	VSS_208	K20
AF37	VSS_29	VSS_118	AN8	VSS_209	K23
AF40	VSS_30	VSS_119	AN9	VSS_210	K26
AF5	VSS_31	VSS_120	AN9	VSS_211	K33
AF6	VSS_32	VSS_121	AP1	VSS_212	K35
AF7	VSS_33	VSS_122	AP11	VSS_213	K37
AG36	VSS_34	VSS_123	AP14	VSS_214	K39
AH2	VSS_35	VSS_124	AP17	VSS_215	K6
AH3	VSS_36	VSS_125	AP22	VSS_216	L10
AH33	VSS_37	VSS_126	AP25	VSS_217	L17
AH36	VSS_38	VSS_127	AP27	VSS_218	L20
AH37	VSS_39	VSS_128	AP36	VSS_219	L23
AH38	VSS_40	VSS_129	AP37	VSS_220	L26
AH39	VSS_41	VSS_130	AP4	VSS_221	L29
AH40	VSS_42	VSS_131	AP40	VSS_222	M1
AH5	VSS_43	VSS_132	AP5	VSS_223	M17
AH8	VSS_44	VSS_133	AR11	VSS_224	M2
AJ12	VSS_45	VSS_134	AR14	VSS_225	M20
AJ15	VSS_46	VSS_135	AR17	VSS_226	M23
AJ18	VSS_47	VSS_136	AR18	VSS_227	M26
AJ21	VSS_48	VSS_137	AR19	VSS_228	M29
AJ25	VSS_49	VSS_138	AR27	VSS_229	M33
AJ27	VSS_50	VSS_139	AR30	VSS_230	M35
AJ36	VSS_51	VSS_140	AR36	VSS_231	M37
AJ5	VSS_52	VSS_141	AR5	VSS_232	M39
AK1	VSS_53	VSS_142	AT1	VSS_233	M42
AK10	VSS_54	VSS_143	AT10	VSS_234	M45
AK13	VSS_55	VSS_144	AT12	VSS_235	M47
AK14	VSS_56	VSS_145	AT13	VSS_236	M49
AK16	VSS_57	VSS_146	AT15	VSS_237	M5
AK22	VSS_58	VSS_147	AT16	VSS_238	M6
AK28	VSS_59	VSS_148	AT17	VSS_239	M9
AK31	VSS_60	VSS_149	AT2	VSS_240	N8
AK32	VSS_61	VSS_150	AT25	VSS_241	P1
AK33	VSS_62	VSS_151	AT27	VSS_242	P2
AK34	VSS_63	VSS_152	AT28	VSS_243	P36
AK35	VSS_64	VSS_153	AT29	VSS_244	P38
AK36	VSS_65	VSS_154	AT3	VSS_245	P40
AK37	VSS_66	VSS_155	AT30	VSS_246	P5
AK4	VSS_67	VSS_156	AT31	VSS_247	P6
AK40	VSS_68	VSS_157	AT32	VSS_248	P33
AK5	VSS_69	VSS_158	AT33	VSS_249	P35
AK6	VSS_70	VSS_159	AT34	VSS_250	P37
AK7	VSS_71	VSS_160	AT35	VSS_251	P39
AK8	VSS_72	VSS_161	AT36	VSS_252	P8
AK9	VSS_73	VSS_162	AT37	VSS_253	T1
AL11	VSS_74	VSS_163	AT38	VSS_254	T5
AL14	VSS_75	VSS_164	AT39	VSS_255	T6
AL17	VSS_76	VSS_165	AT4	VSS_256	U8
AL19	VSS_77	VSS_166	AT40	VSS_257	V1
AL24	VSS_78	VSS_167	AT5	VSS_258	V2
AL27	VSS_79	VSS_168	AT6	VSS_259	V33
AL30	VSS_80	VSS_169	AT7	VSS_260	V34
AL36	VSS_81	VSS_170	AT8	VSS_261	V35
AL5	VSS_82	VSS_171	AT9	VSS_262	V36
AM1	VSS_83	VSS_172	AU1	VSS_263	V37
AM11	VSS_84	VSS_173	AU15	VSS_264	V38
AM14	VSS_85	VSS_174	AU26	VSS_265	V39
AM17	VSS_86	VSS_175	AU34	VSS_266	V40
AM2	VSS_87	VSS_176	AU4	VSS_267	V5
AM21	VSS_88	VSS_177	AU6	VSS_268	W6
AM23	VSS_89	VSS_178	AU8	VSS_269	Y5
AM25	VSS_90	VSS_179	AV10	VSS_270	Y8
A4	VSS_91	VSS_180	AV39	VSS_271	B3
VSS_NCTF_1 VSS_NCTF_2			VSS_NCTF_3 VSS_NCTF_4		

DE NOTE:
DQ VREF OPTION 1 - VOLTAGE DIVIDER GENERATED -- Page 8
DQ VREF OPTION 2 - PROGRAMMABLE DAC GENERATED -- Removed
DQ VREF OPTION 3 - CPU GENERATED -- This Page
TO MAINTAIN CONSISTENCY
AH4 FOR CHANNEL A DDR_VREF, AH1 FOR CHANNEL B

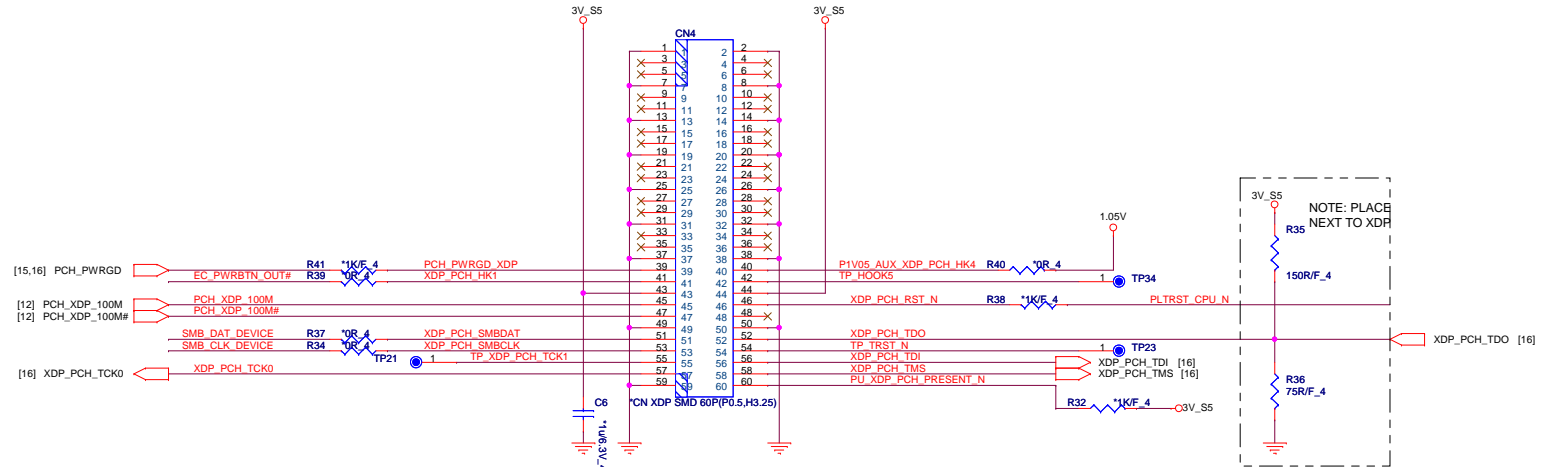


DE NOTE:
STUFF ALL FOUR EMPTY RESISTOR AND THE UPSTREAM ONE TO USE CPU VREF DQ B TO DRIVE VREF CA A AND B
NEED TO UNSTUFF THE APPROPRIATE RESISTORS ON PAGE 16 AND 17
STUFF THE LOWER THREE EMPTY RESISTOR TO USE DIG. POT. VREF DQ B TO DRIVE VREF CA A AND B
NEED TO UNSTUFF THE APPROPRIATE RESISTORS ON PAGE 16 AND 17

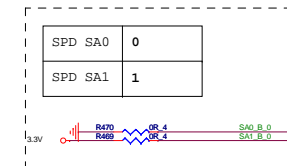
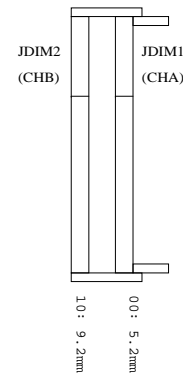
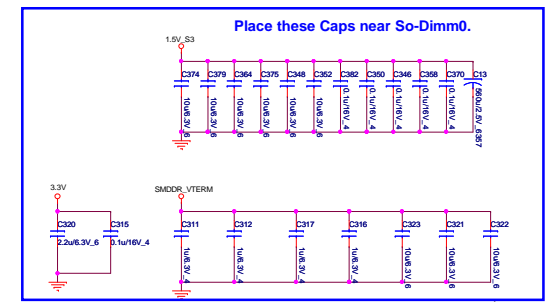
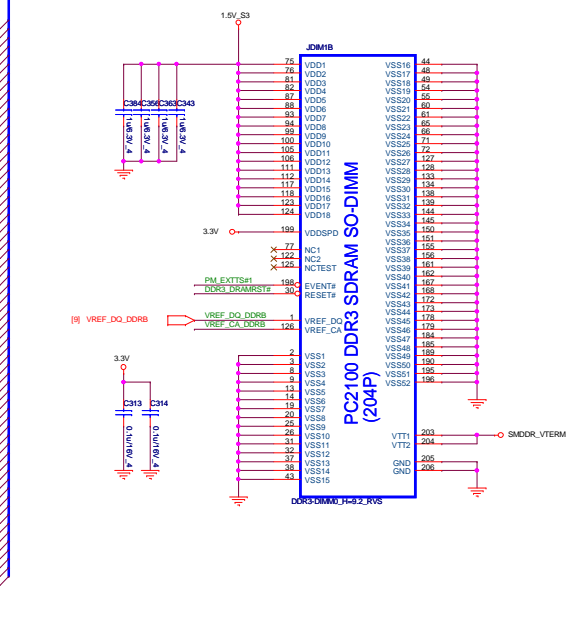
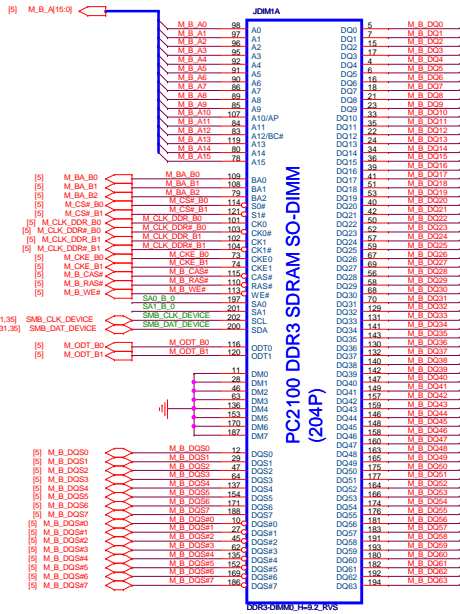


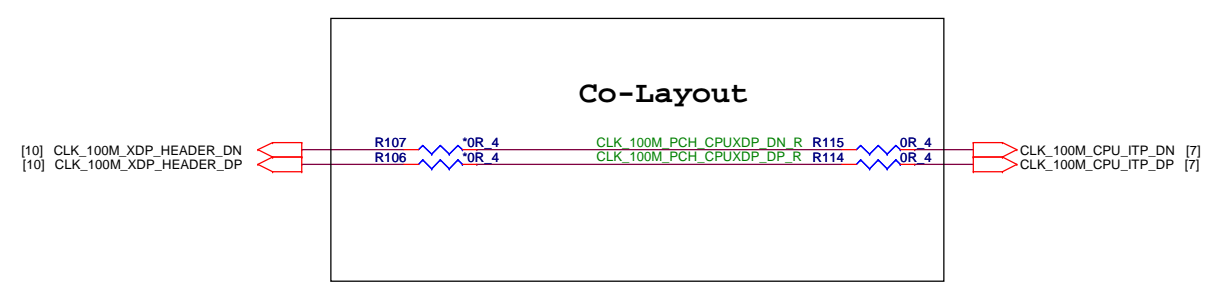
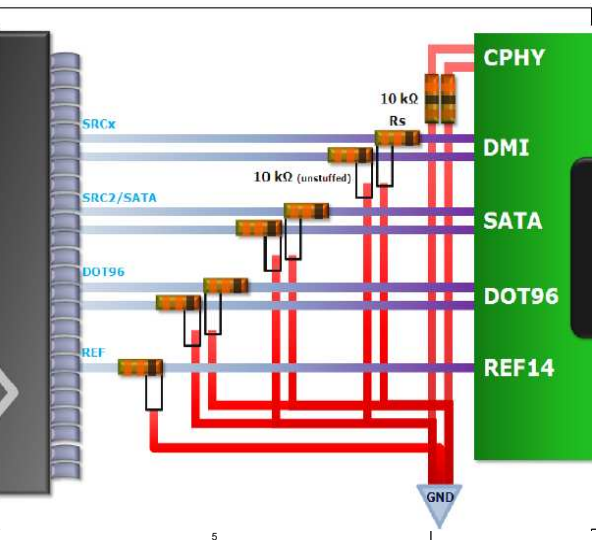
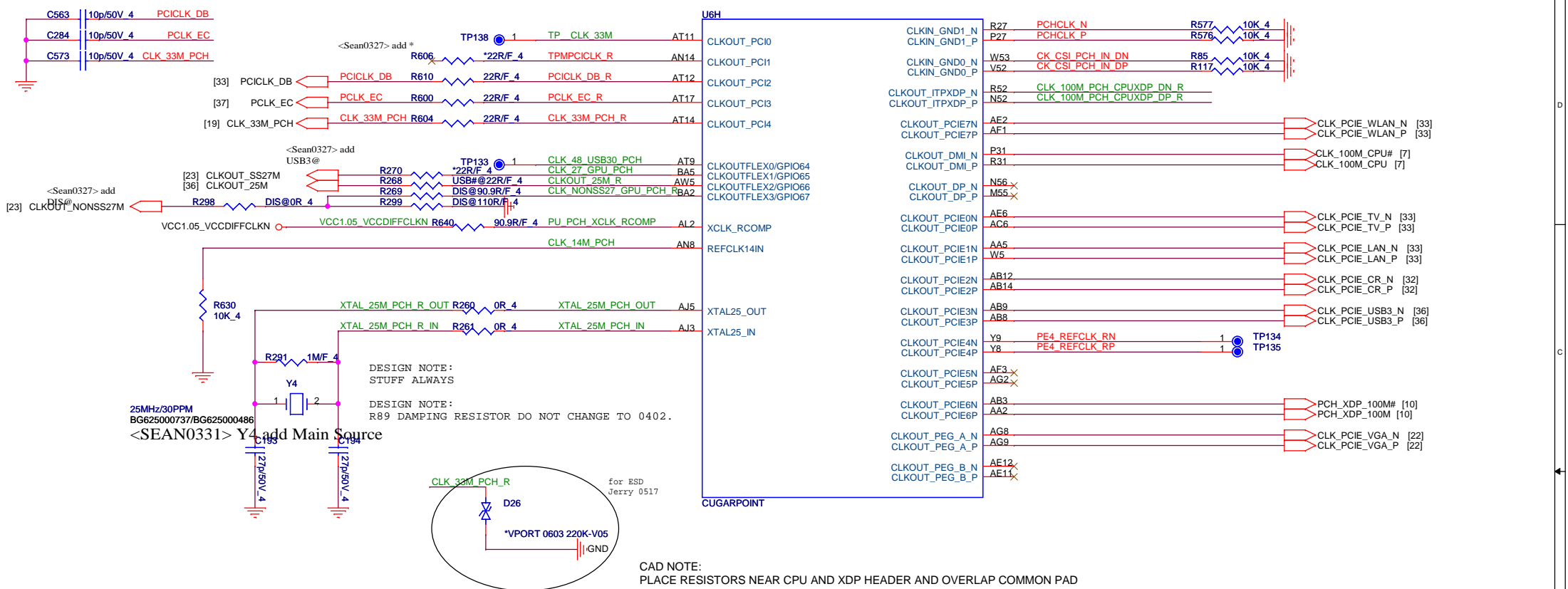


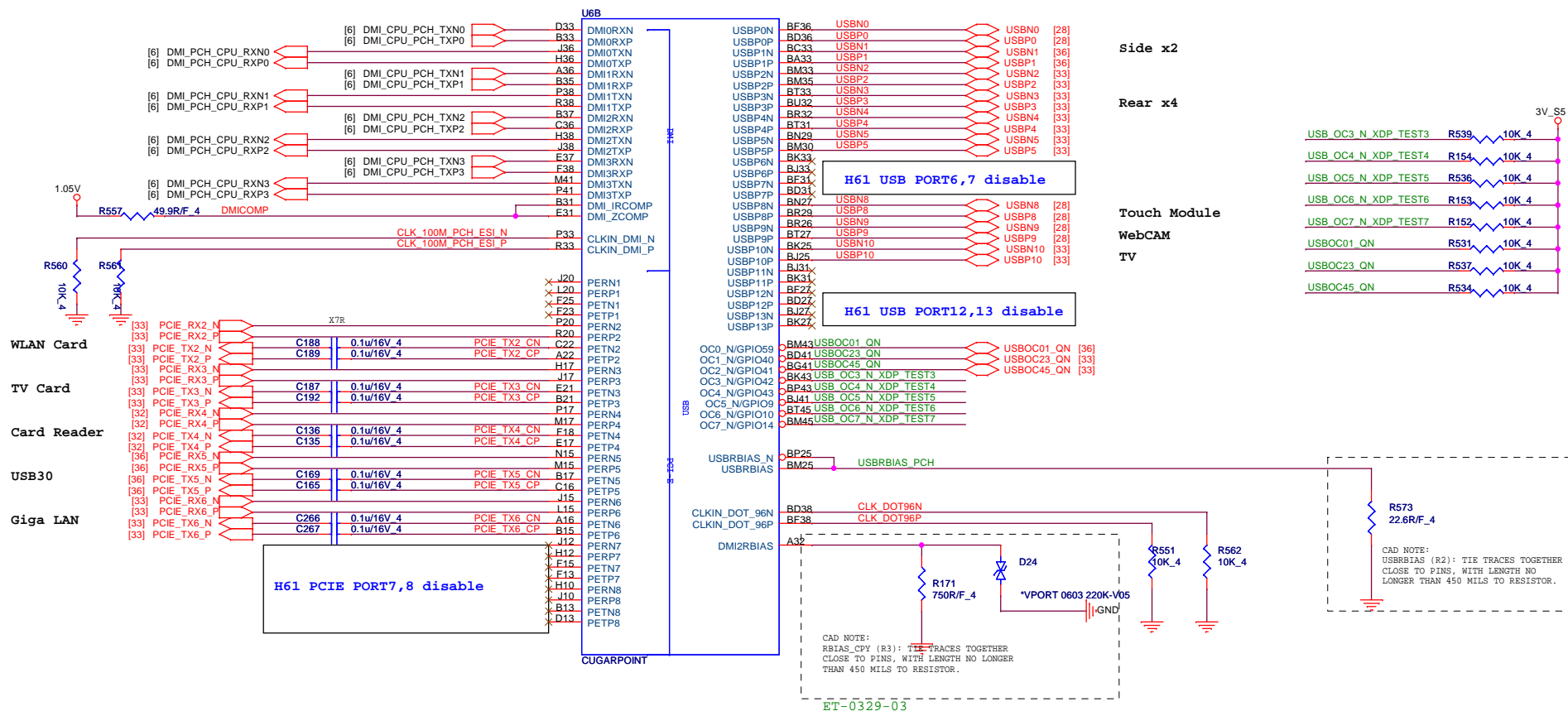
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CHANNEL B DIMM 2

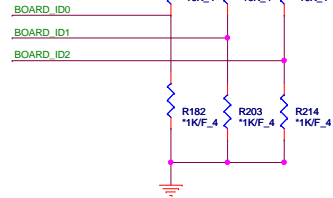




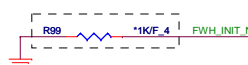
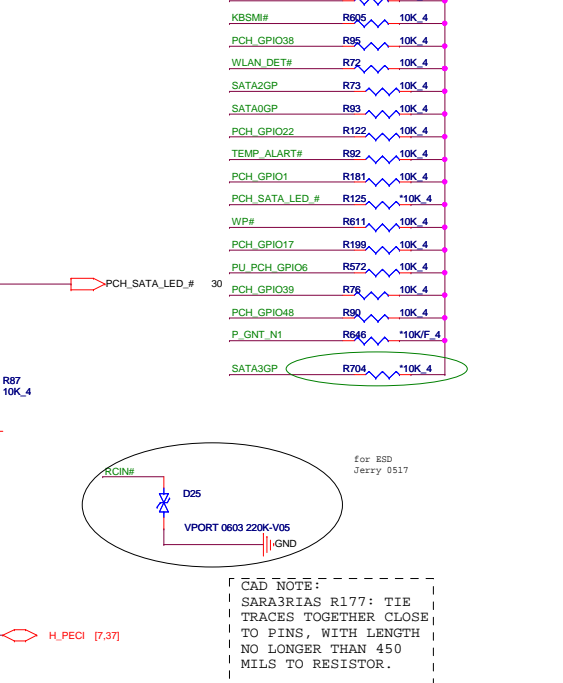
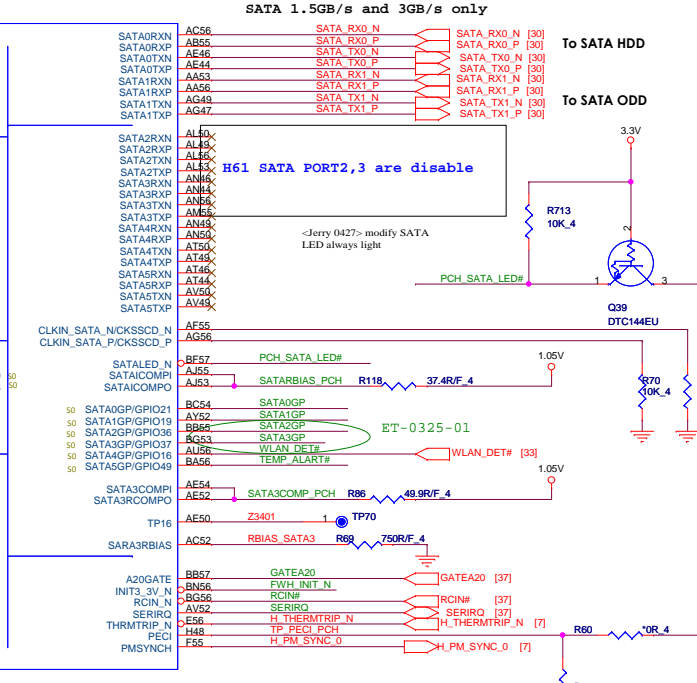
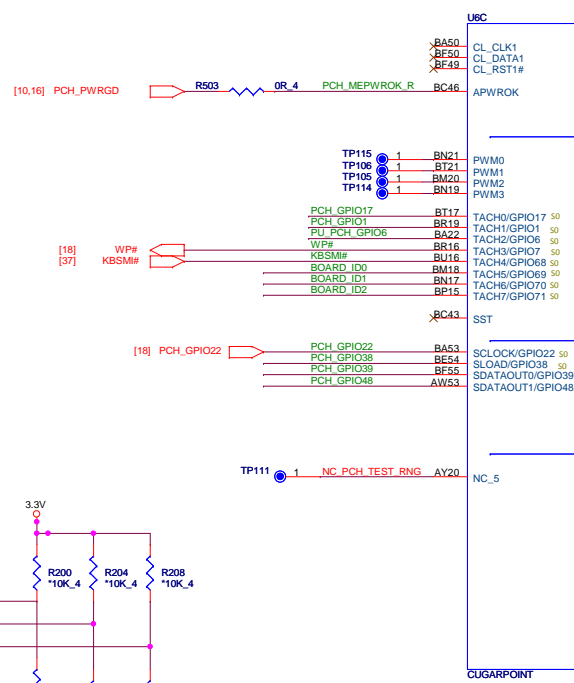


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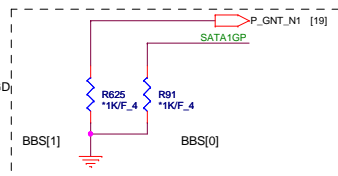
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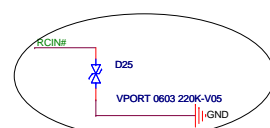
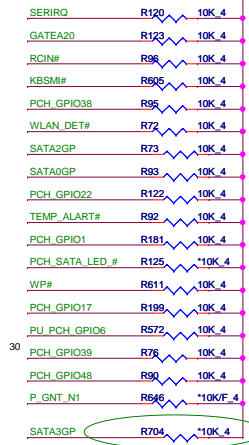
<Sean0327> remove Board ID table



DESIGN NOTE:
CPU OUTPUT BUFFER STRENGTH FOR CPU_PWD[0]
AND PM_SYNC
P/U: STANDARD STRENGTH (DEFAULT)
P/D: STRONGER STRENGTH
PCH PROVIDES WEAK INTERNAL P/U



DESIGN NOTE:
BIOS BOOT DEVICE STRAP
1 1 SPI (DEFAULT)
1 0 PCI
0 1 RESERVED
0 0 LPC
PCH PROVIDES WEAK INTERNAL P/U



for BSD
Jerry 0517

CAD NOTE:
SARA3RIAS R177: TIE
TRACES TOGETHER CLOSE
TO PINS, WITH LENGTH
NO LONGER THAN 450
MILS TO RESISTOR.

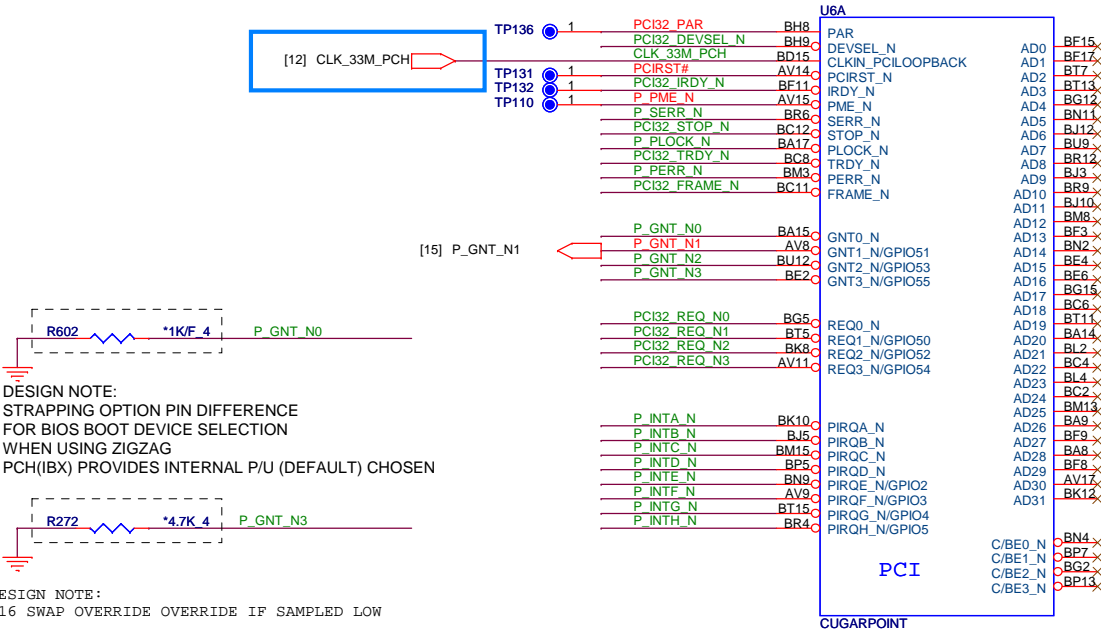
CAD NOTE:
SATA3COMP_PCH R176: TIE
TRACES TOGETHER CLOSE
TO PINS, WITH LENGTH NO
LONGER THAN 200 MILS TO
RESISTOR.

CAD NOTE:
SATA3_RBIAS R177:
ROUTE TRACE LENGTH
NO LONGER THAN 450
MILS TO RESISTOR.

Pin No	Pin name	NET	Type	Tolerance	Power Well	Default	Function Description	HW
AW55	GPIO0 / BMBUSY#	BMBUSY#	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BR19	GPIO1 / TACH1	PCH_GPIO1	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BN9	GPIO2 / PIRQ[E]#	P_INTE_N	I/O	5V	Core	GPI	GPIO	PU 8.2K to 3.3V
AV9	GPIO3 / PIRQ[F]#	P_INTF_N	I/O	5V	Core	GPI	GPIO	PU 8.2K to 3.3V
BT15	GPIO4 / PIRQ[G]#	P_INTG_N	I/O	5V	Core	GPI	GPIO	PU 8.2K to 3.3V
BR4	GPIO5 / PIRQ[H]#	P_INTH_N	I/O	5V	Core	GPI	GPIO	PU 8.2K to 3.3V
BA22	GPIO6 / TACH2	PU_PCH_GPIO6	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BR16	GPIO7 / TACH3	WP#	I/O	3.3V	Core	GPI	GPO, BIOS WP#(reserved)	PU 10K to 3.3V
BP51	GPIO8	SEL_FCIM_EN	I/O	3.3V	Suspend	GPO	GPI, Select FCIM Enable	PD 1K to GND
BJ41	GPIO9 / OC5#	USB_OC5_N_XDP_TEST5	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BT45	GPIO10 / OC6#	USB_OC6_N_XDP_TEST6	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BN49	GPIO11 / SMBALERT#	IRQ_PCH_NMI_N	I/O	3.3V	Suspend	Native	Non-Maskable Interrupt	PU 10K to 3V_S5
BK50	GPIO12 / LAN_PHY_PWR_CTRL	SCI#	I/O	3.3V	Suspend	Native	GPI as SCI#	EC
BA25	GPIO13	PCH_GPIO13	I/O	3.3V	Suspend	GPI	GPIO	PU 10K to 3V_S5
BM45	GPIO14 / OC7#	USB_OC7_N_XDP_TEST7	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BM55	GPIO15	SEL_TL5_EN	I/O	3.3V	Suspend	GPO	Strapping Pin. TL5Confidentiality (internal PL)	PU 10K to 3V_S5
AJ56	GPIO16 / SATA4GP	WLAN_DET#	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BT17	GPIO17 / TACH0	PCH_GPIO17	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
GPIO18 (Mobile Only)								
AY52	GPIO19 / SATA1GP	SATA1GP	I/O	3.3V	Core	GPI	Strapping Pin. Boot BIOS Strap	
AV43	GPIO20 / PCIECLKRQ2#/SMI#	CR_CLK_REQ#_R#	I/O	3.3V	Core	Native	GPIO	PU 10K to 3.3V
BC54	GPIO21 / SATA0GP	SATA0GP	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BA53	GPIO22 / SCLOCK	PCH_GPIO22	I/O	3.3V	Core	GPI	GPI, recovery BIOS	PU 10K to 3.3V
BA20	GPIO23 / LDRQ1#	L_DRQ1_N	I/O	3.3V	Core	Native	GPO	
BP53	GPIO24	USB30_SMI#_PCH	I/O	3.3V	Suspend	GPO	GPI, USB3.0_SMI#(reserved)	PU 10K to 3V_S5
GPIO25 / PCIECLKRQ3# (Mobile Only)								
GPIO26 / SA_STATES (Mobile Only)								
BJ43	GPIO27	Not Connect	I/O	3.3V	DSW	GPI	GPO, (internal PU 20K 3V_S5)	
BJ55	GPIO28	OD_PLLVR_GPIO28	I/O	3.3V	Suspend	GPO	GPI, Strapping Pin. On-Die PLL VR (internal PU)	
BH49	GPIO29 / SLP_LAN#	N54128069	I/O	3.3V	Suspend	GPI	GPO	TP68
BJ46	GPIO30 / SUSPWRDNACK/SUSWARN#	SUSWARN#	I/O	3.3V	Suspend	Native	native	PU 10K to 3V_S5
BG43	GPIO31 / OC77#	GPIO31	I/O	3.3V	DSW	GPI	GPIO	PU 10K to 3V_S5
BC56	GPIO32	CLKRUN_N_R	I/O	3.3V	Core	GPO	GPO	TP65
BC25	GPIO33	WRITE_EDID_ROM	I/O	3.3V	Core	GPO	High-SMBUS access EDID enable, Low: default	PU 10K to 3.3V
BL56	GPIO34 / STP_PCI#	STP_PCI_N	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BJ57	GPIO35 / NMI#	PECI_REQ_#	I/O	3.3V	Core	GPO	GPIO	PU 10K to 3V_S5
BB55	GPIO36 / SATA2GP	SATA2GP	I/O	3.3V	Core	GPI	Strapping Pin. Reserved (internal PL)	PU 10K to 3.3V
BG53	GPIO37 / SATA3GP	SATA3GP	I/O	3.3V	Core	GPI	GPO	
BE54	GPIO38 / SLOAD	PCH_GPIO38	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BF55	GPIO39 / SDATAOUT0	PCH_GPIO39	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BD41	GPIO40 / OC11#	USBOC23_QN	I/O	3.3V	Suspend	Native	USB OC1	PU 10K to 3V_S5
BG41	GPIO41 / OC12#	USBOC45_QN	I/O	3.3V	Suspend	Native	USB OC2	PU 10K to 3V_S5
BK43	GPIO42 / OC13#	USB_OC3_N_XDP_TEST3	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BP43	GPIO43 / OC14#	USB_OC4_N_XDP_TEST4	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BL54	GPIO44 / PCIECLKRQ5#	LAN_CLK_REQ#	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
AV44	GPIO45 / PCIECLKRQ6#	PCH_GPIO45	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BP55	GPIO46 / PCIECLKRQ7#	PCH_GPIO46	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
GPIO47 / SATA5GP (Mobile Only)								
AW53	GPIO48 / SDATAOUT1	PCH_GPIO48	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BA56	GPIO49 / SATA5GP/TEMP_ALERT#	TEMP_ALERT#	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BT5	GPIO50 / REQ1#	PCI32_REQ_N1	I/O	5V	Core	Native	GPIO	PU 8.2K to 3.3V
AV8	GPIO51 / GNT1#	P_GNT_N1	I/O	3.3V	Core	Native	GPO, Strapping Pin. Boot BIOS Strap	
BK8	GPIO52 / REQ2#	PCI32_REQ_N2	I/O	5V	Core	Native	GPIO	PU 8.2K to 3.3V
BU12	GPIO53 / GNT2#	P_GNT_N2	I/O	3.3V	Core	Native	GPO, This signal should not be pulled low for desktop and mobile(internal PU)	
AV11	GPIO54 / REQ3#	PCI32_REQ_N3	I/O	5V	Core	Native	GPIO	PU 8.2K to 3.3V
BE2	GPIO55 / GNT3#	P_GNT_N3	I/O	3.3V	Core	Native	GPO, Strapping Pin. Top-Block Swap Override	
GPIO56 / SML1ALERT# (Mobile Only)								
BT53	GPIO57	Not Connect	I/O	3.3V	Suspend	GPI	GPO	
BJ46	GPIO58 / SML1CLK	SML1CLK_PCH	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BM43	GPIO59 / OC10#	USBOC01_QN	I/O	3.3V	Suspend	Native	USB OC0	PU 10K to 3V_S5
BU49	GPIO60 / SML0ALERT#	SMLALERT_PCH	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BN54	GPIO61 / SUS_STAT#	LPCPD_N	I/O	3.3V	Suspend	Native	GPO	TP64
BA47	GPIO62 / SUSCLK	PCH_SUSCLK	I/O	3.3V	Suspend	Native	GPO	TP75
BH50	GPIO63 / SLP_S5#	TP_SLP_S5_N	I/O	3.3V	Suspend	Native	GPO	TP67
AT9	GPIO64 / CLKOUTFLEX0	CLK_48_USB30_PCH	I/O	3.3V	Core	Native	GPO	TP133
BA5	GPIO65 / CLKOUTFLEX1	CLK_27_GPU_PCH	I/O	3.3V	Core	Native	CLK27M	GPU
AW5	GPIO66 / CLKOUTFLEX2	CLKOUT_25M_R	I/O	3.3V	Core	Native	CLK25M	USB3.0
BA2	GPIO67 / CLKOUTFLEX3	CLK_NONSS27_GPU_PCH_R	I/O	3.3V	Core	Native	CLK27M	GPU
BU16	GPIO68 / TACH4	KBSMI#	I/O	3.3V	Core	GPI	SMI	PU 10K to 3.3V
BM18	GPIO69 / TACH5	BOARD_ID0	I/O	3.3V	Core	GPI	GPIO	PU 10K to 3.3V
BN17	GPIO70 / TACH6	BOARD_ID1	I/O	3.3V	Core	Native	GPIO	PU 10K to 3.3V
BP15	GPIO71 / TACH7	BOARD_ID2	I/O	3.3V	Core	Native	GPIO	PU 10K to 3.3V
AV46	GPIO72	PU_PCH_GP72	I/O	3.3V	Suspend	Native	GPI, Desktop: Unmultiplexed; requires pull-up resistor.	PU 10K to 3V_S5
GPIO73 / SML1ALERT# (Mobile Only)								
BR46	GPIO74 / SML1ALERT#/PCHHOT#	SML1ALERT_PCH	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5
BK46	GPIO75 / SML1DATA	SML1DATA_PCH	I/O	3.3V	Suspend	Native	GPIO	PU 10K to 3V_S5

<Scan0327> modify V2.0

Layout note:
Loopback length and clock-to-device length must be within maximum 5000-mil delta to meet Tskew requirement



DESIGN NOTE:
STRAPPING OPTION PIN DIFFERENCE
FOR BIOS BOOT DEVICE SELECTION
WHEN USING ZIGZAG
PCH(IBX) PROVIDES INTERNAL P/U (DEFAULT) CHOSEN

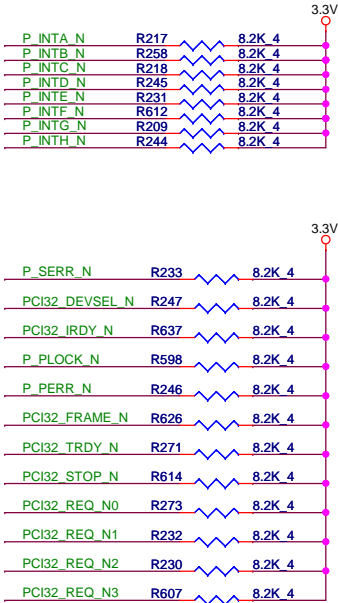
DESIGN NOTE:
A16 SWAP OVERRIDE OVERRIDE IF SAMPLED LOW

GNT2/GPIO53:
ESI Strap (Server Only)
ESI compatible mode is for server
platforms only. This signal should
not be pulled low for desktop and
mobile.

PCI Interface termination requirement

Signal Name	Type	Termination Requirement
AD[31:0]	I/O	Can be left unconnected.
C/BE[3:0]#	I/O	Can be left unconnected.
DEVSEL#	I/O	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.
FRAME#	I/O	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.
IRDY#	I/O	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.
TRDY#	I/O	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.

PCI PULL-UPS



PCI Interface termination requirement

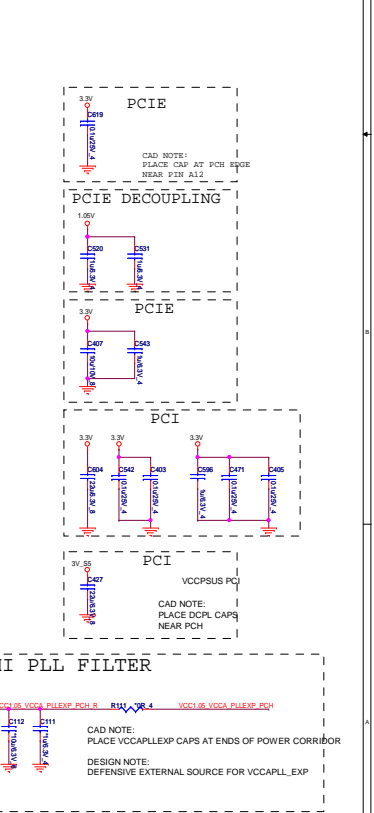
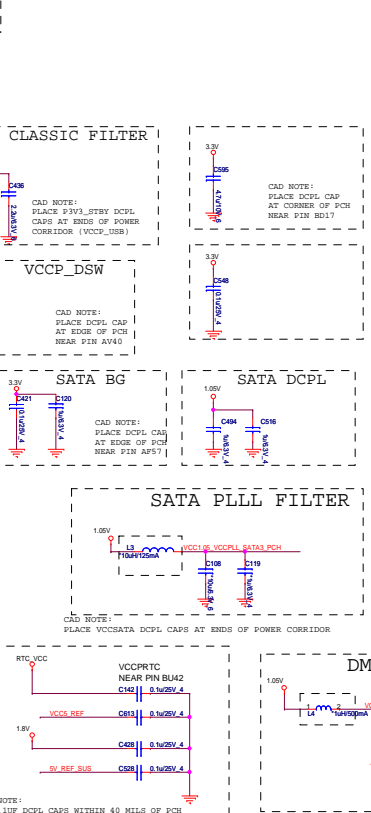
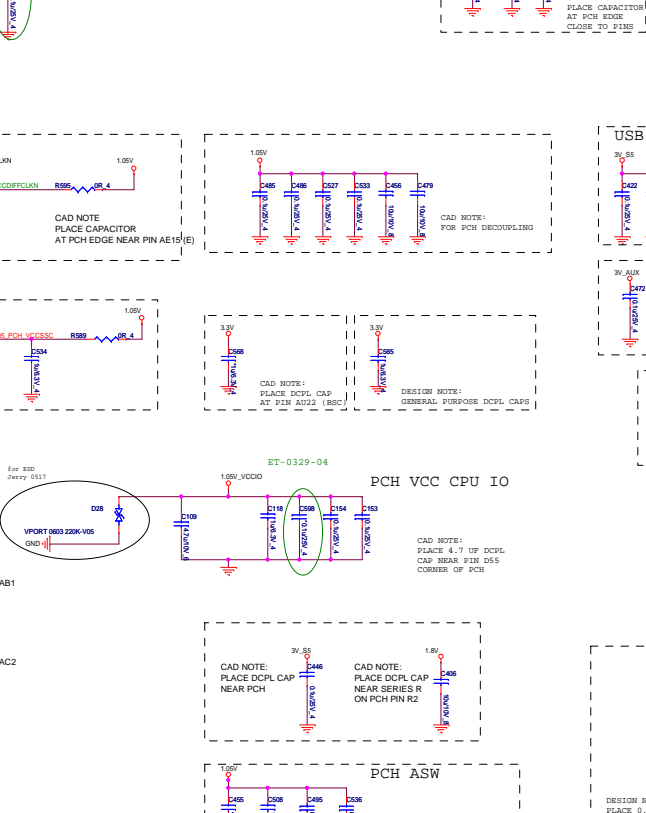
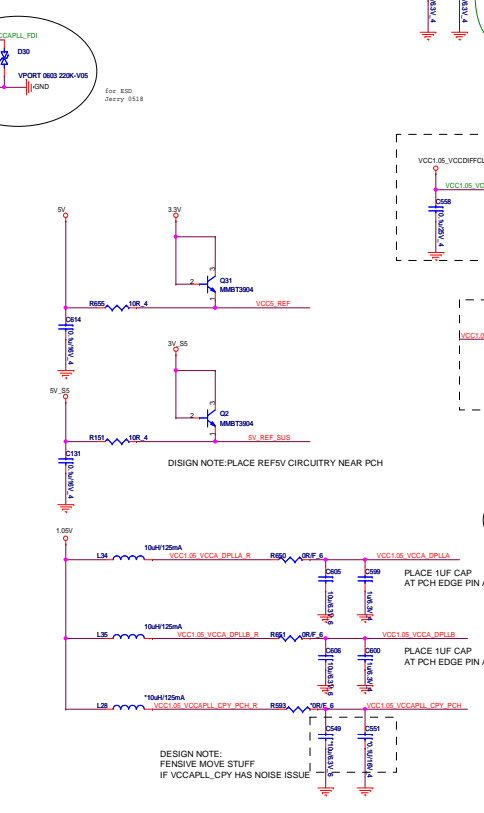
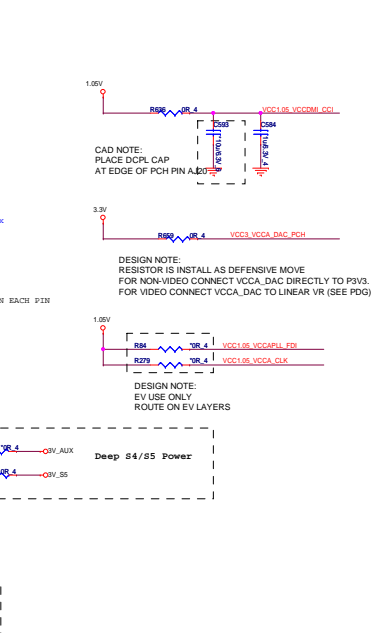
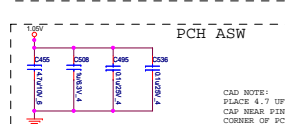
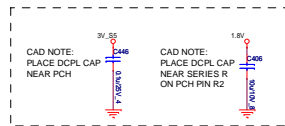
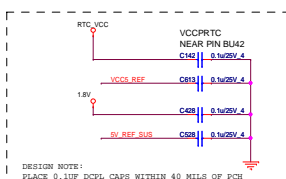
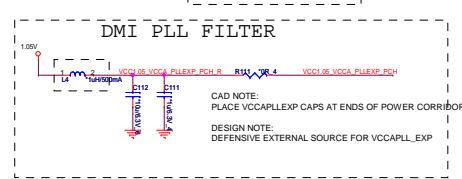
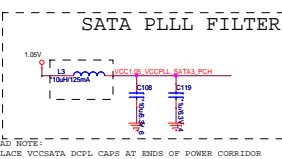
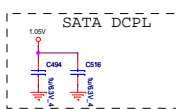
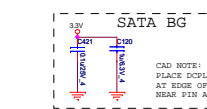
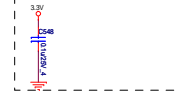
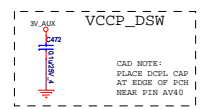
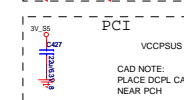
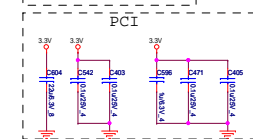
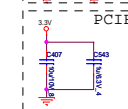
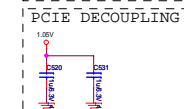
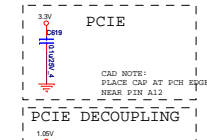
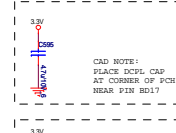
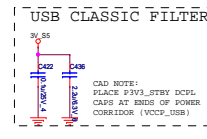
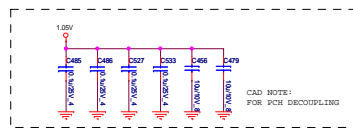
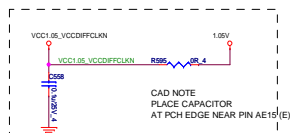
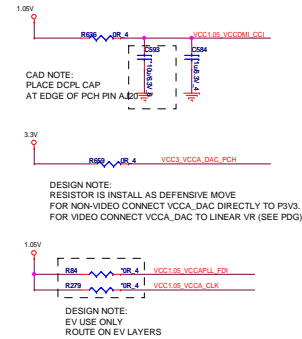
Signal Name	Type	Termination Requirement
STOP#	I/O	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.
PAR	I/O	Can be left unconnected.
PERR#	I/O	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.
REQ[3:0]#	I	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3. REQ[3:1] can be configured as GPIO instead.
GNT[3:0]#	O	Can be left unconnected. GNT[3:1]# can be configured as GPIO instead. GNT[3:0] is sampled as a functional strapping, refer to PCH EDS for strapping requirement.
PCICLK	I	Need to remain connected to 33MHz clock source.
PCIRST#	O	Can be left unconnected.
PLOCK#	I/O	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.
SERR#	I/OD	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.
PME#	I/OD	Can be left unconnected. Internally pull up.
PIRQ[D:A]#	I/OD	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3.
PIRQ[H:E]#	I/OD	Requires a 8.2k Ohm weak pull-up resistor to Vcc3_3. Can be configured as GPIO instead.

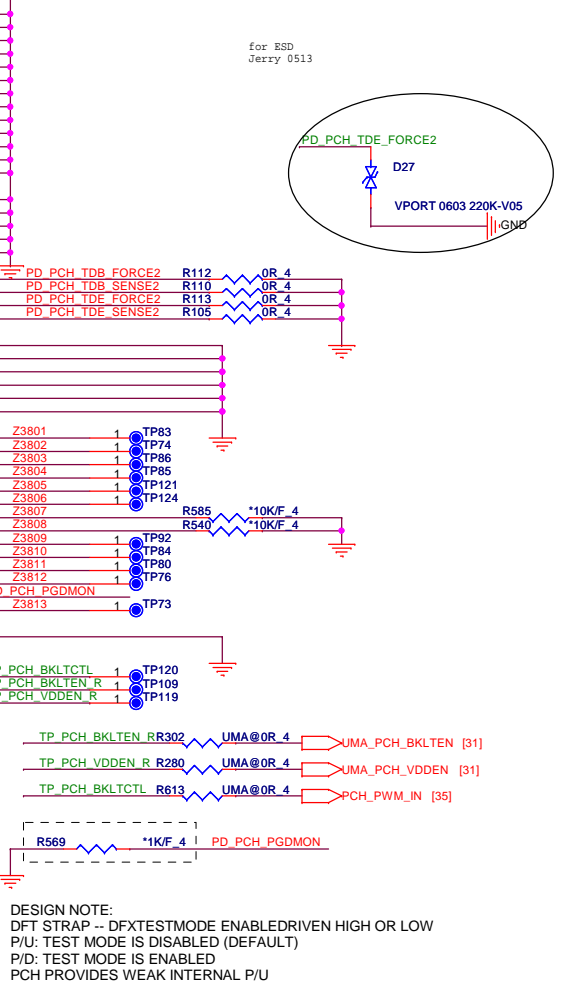
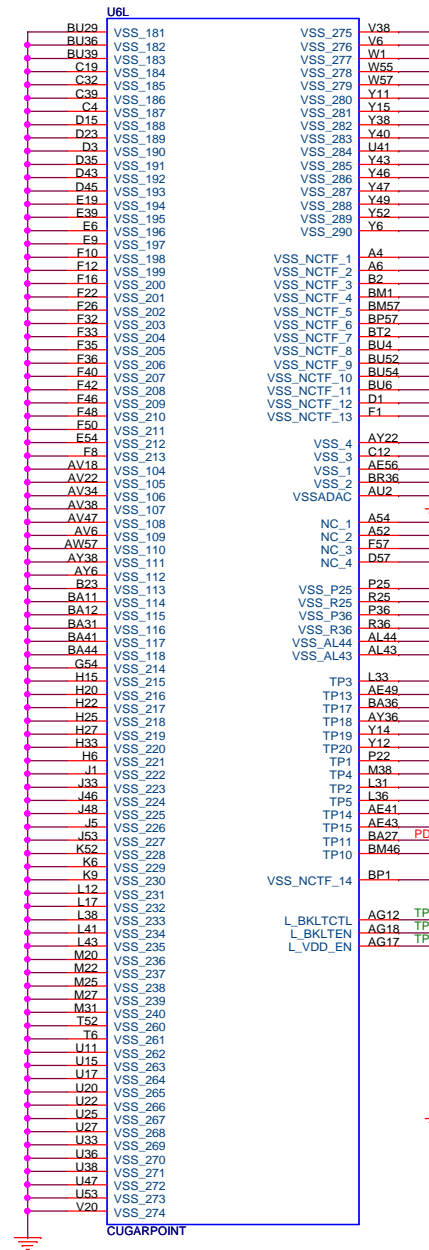
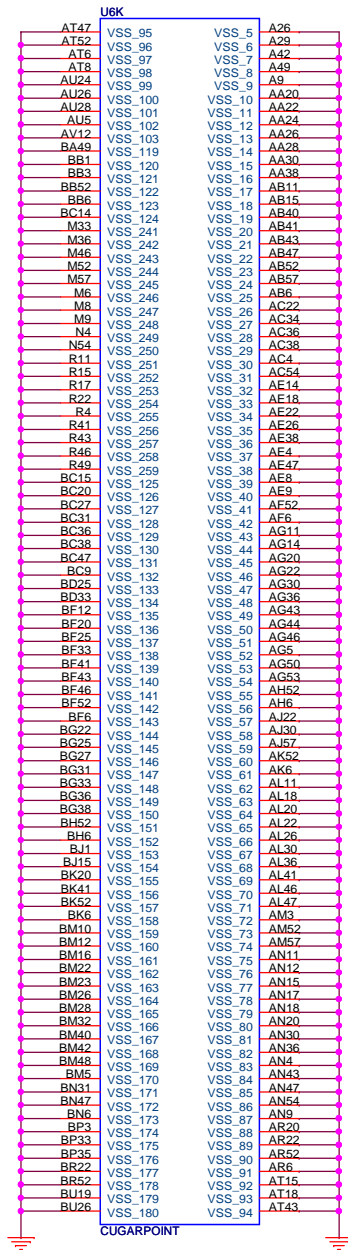
PME# Internal PU
3V_S5

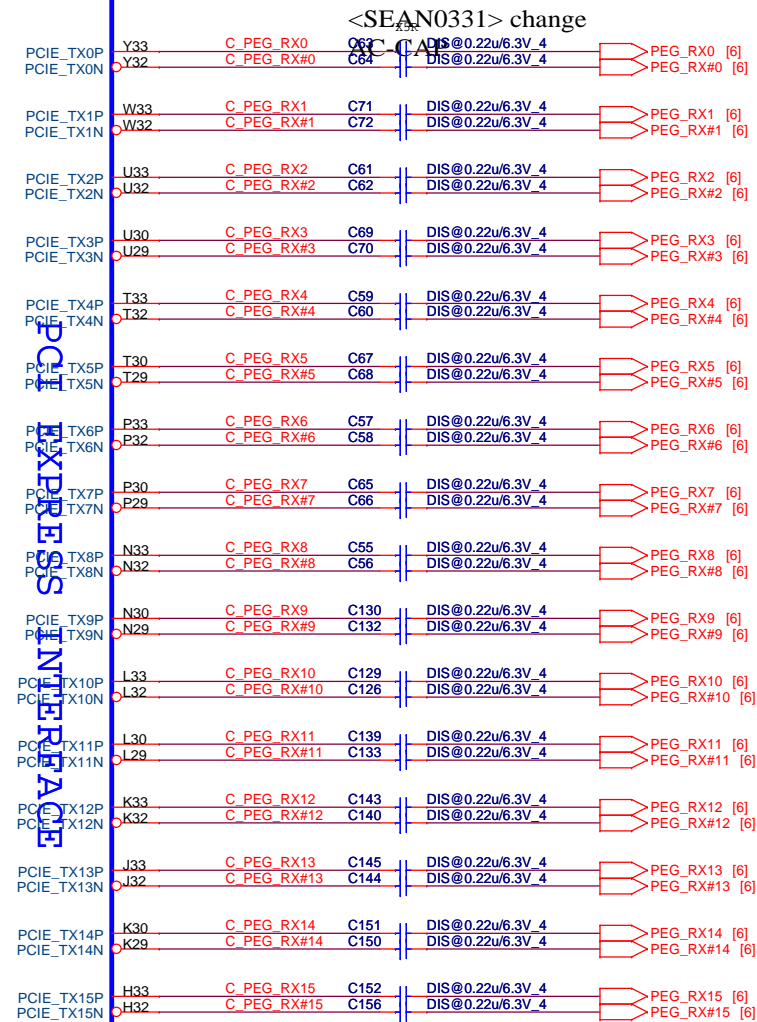
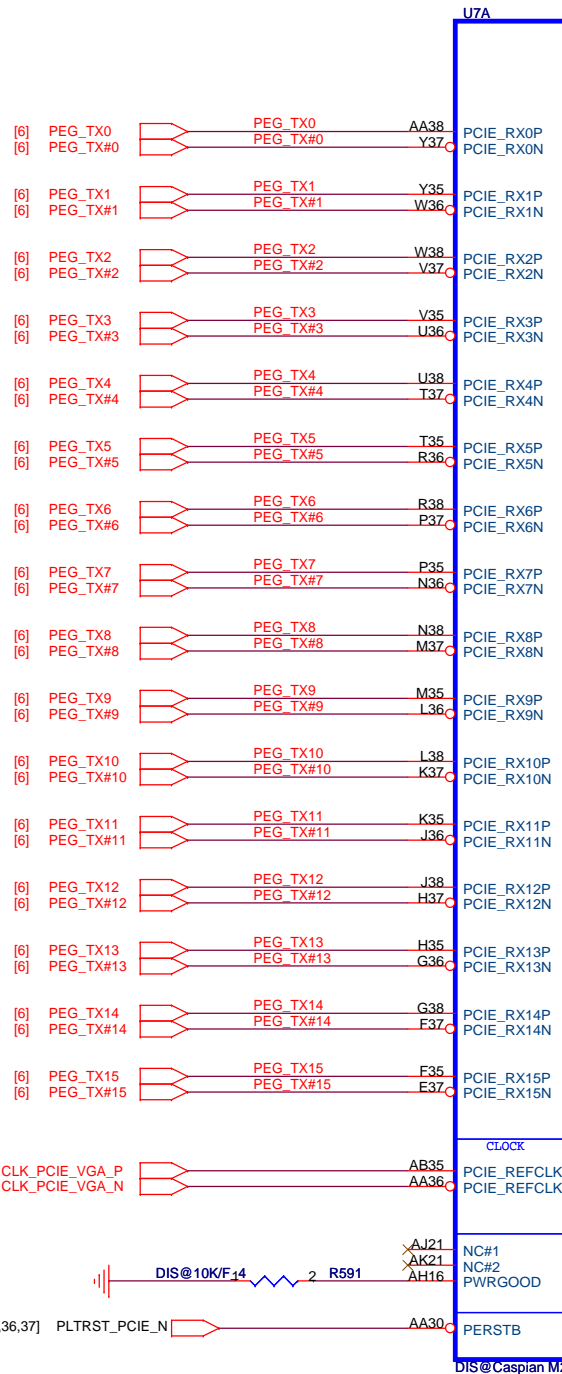


Quanta Computer Inc.
PROJECT : QUA

Size	Document Number	Rev
	PCH_PCI	1A
Date:	Monday, July 04, 2011	Sheet 19 of 48







Quanta Computer Inc.

PROJECT : QUA

Size	Document Number	Rev
	Caspian_PEG	1A
Date: Monday, July 03, 2011	Sheet 22 of 48	

3V_VGA

<cent>0327> modify

Memory ID

VRAM TYPE

R215 VRAM_DS10KF_4

R216 VRAM_DS10KF_4

R219 VRAM_DS10KF_4

R210 VRAM_DS10KF_4

R200 *DS10KF_4 GFX_CORE_CNTRL0

R202 *DS10KF_4 GFX_CORE_CNTRL0

R197 *DS10KF_4 GPIO_23_CLKREQ0

R575 *DS10KF_4 GPIO24_TRSTB

R568 *DS10KF_4 GPIO25_TDI

R566 *DS10KF_4 GPIO27_TMS

R587 *DS10KF_4 GPIO5

R596 *DS10KF_4 EXT_LVDS_B0N

R578 *DS10KF_4 GPIO0

R580 *DS10KF_4 GPIO1

R179 *DS10KF_4 GPIO2

R134 *DS10KF_4 GPIO3_ROMS0

R133 *DS10KF_4 EXT_CRT_HSYNC

R134 *DS10KF_4 EXT_CRT_VSYNC

R603 *DS10KF_4 BSEN

R631 *DS10KF_4 GPIO3_ROMS1

R599 *DS10KF_4 GPIO11

R601 *DS10KF_4 GPIO12

R608 *DS10KF_4 GPIO13

R554 *DS10KF_4 GENCLK_CLK

R631 *DS10KF_4 GPIO22_ROMCS#

VBIOS ROM

3V_VGA

C584 *DS10KF_4

U9

GPIO22_ROMCS#

GPIO3_ROMS0

CE#

ZQ

HOLD#

WP#

VSS

VDD

SCH#

GPIO10_ROMCS#

GPIO3_ROMS1

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GPIO0

GPIO1

GPIO2

GPIO3

GPIO4

GPIO5

GPIO6

GPIO7

GPIO8

GPIO9

GPIO10

GPIO11

GPIO12

GPIO13

GPIO14

GPIO15

GPIO16

GPIO17

GPIO18

GPIO19

GPIO20

GPIO21

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GPIO271

GPIO272

GPIO273

GPIO274

GPIO275

GPIO276

GPIO277

GPIO278

GPIO279

GPIO280

GPIO281

GPIO282

GPIO283

GPIO284

GPIO285

GPIO286

GPIO287

GPIO288

GPIO289

GPIO290

GPIO291

GPIO292

GPIO293

GPIO294

GPIO295

GPIO296

GPIO297

GPIO298

GPIO299

GPIO300

GPIO301

GPIO302

GPIO303

GPIO304

GPIO305

GPIO306

GPIO307

GPIO308

GPIO309

GPIO310

GPIO311

GPIO312

GPIO313

GPIO314

GPIO315

GPIO316

GPIO317

GPIO318

GPIO319

GPIO320

GPIO321

GPIO322

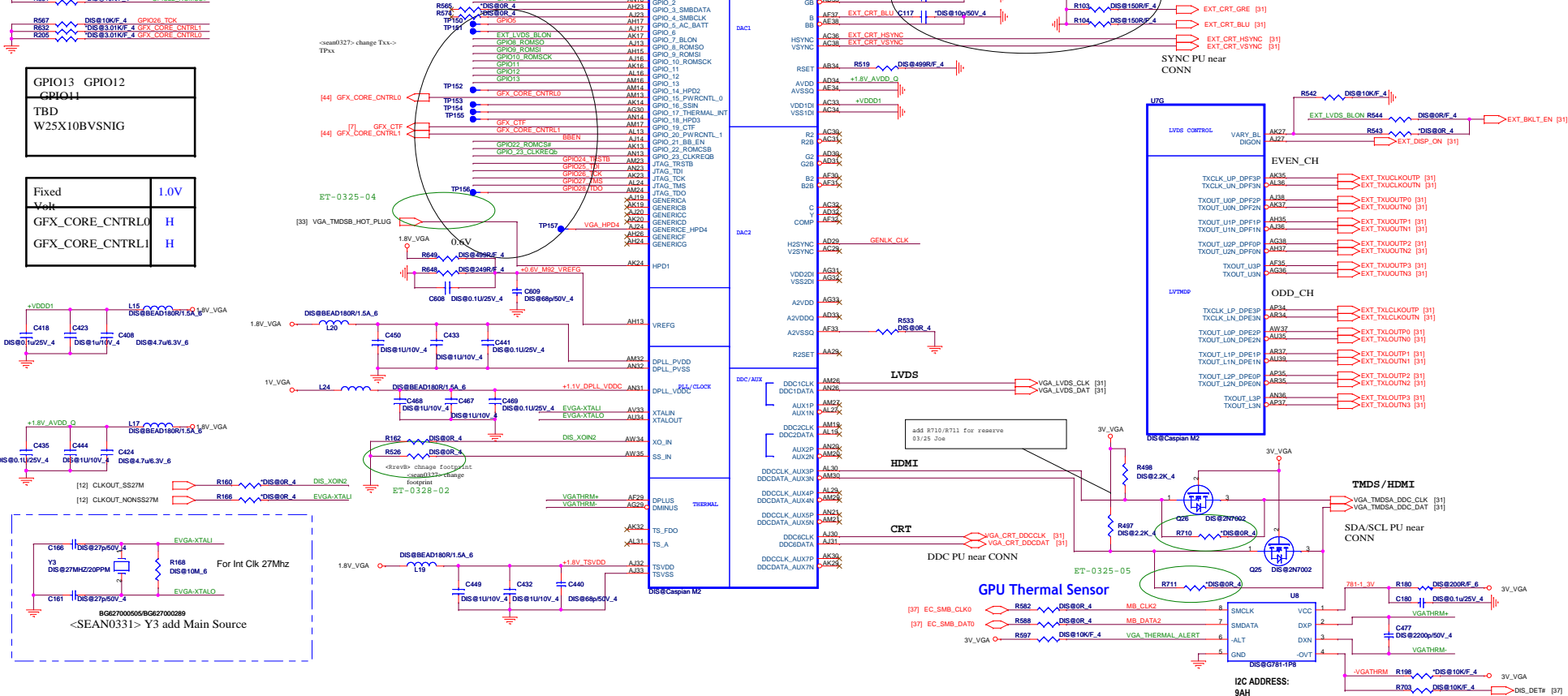
GPIO323

GPIO324

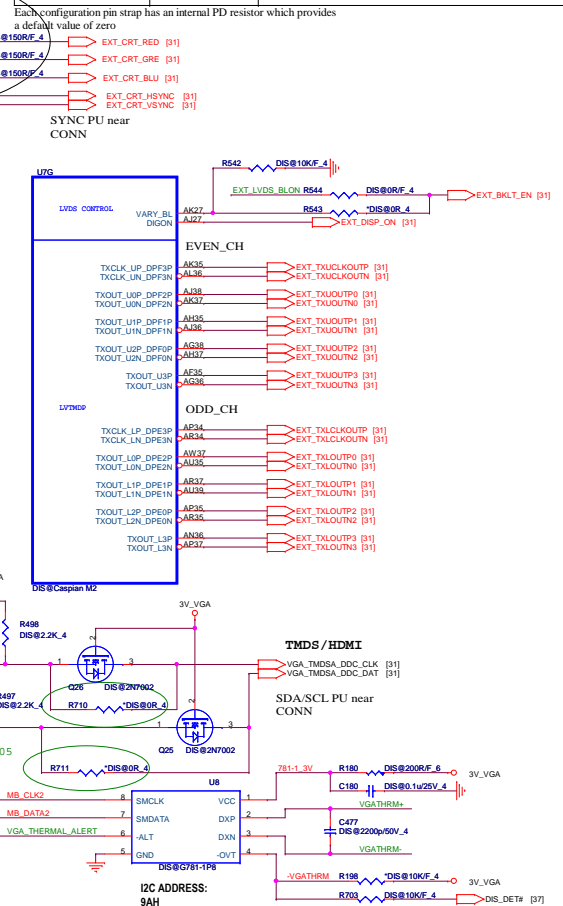
GPIO325

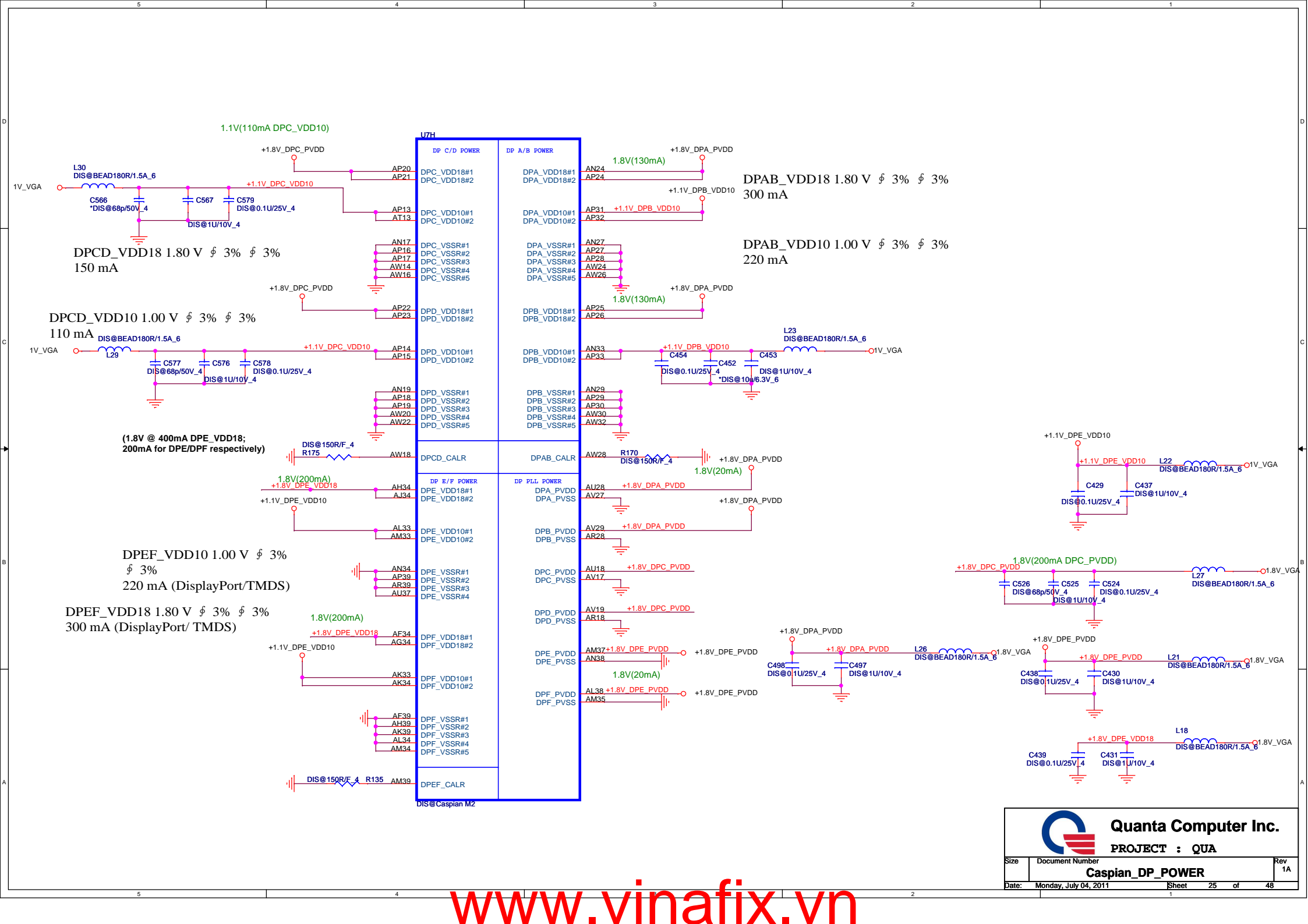
GPIO13 GPIO12 GPIO11	
TBD	
W25X10BVSNIG	

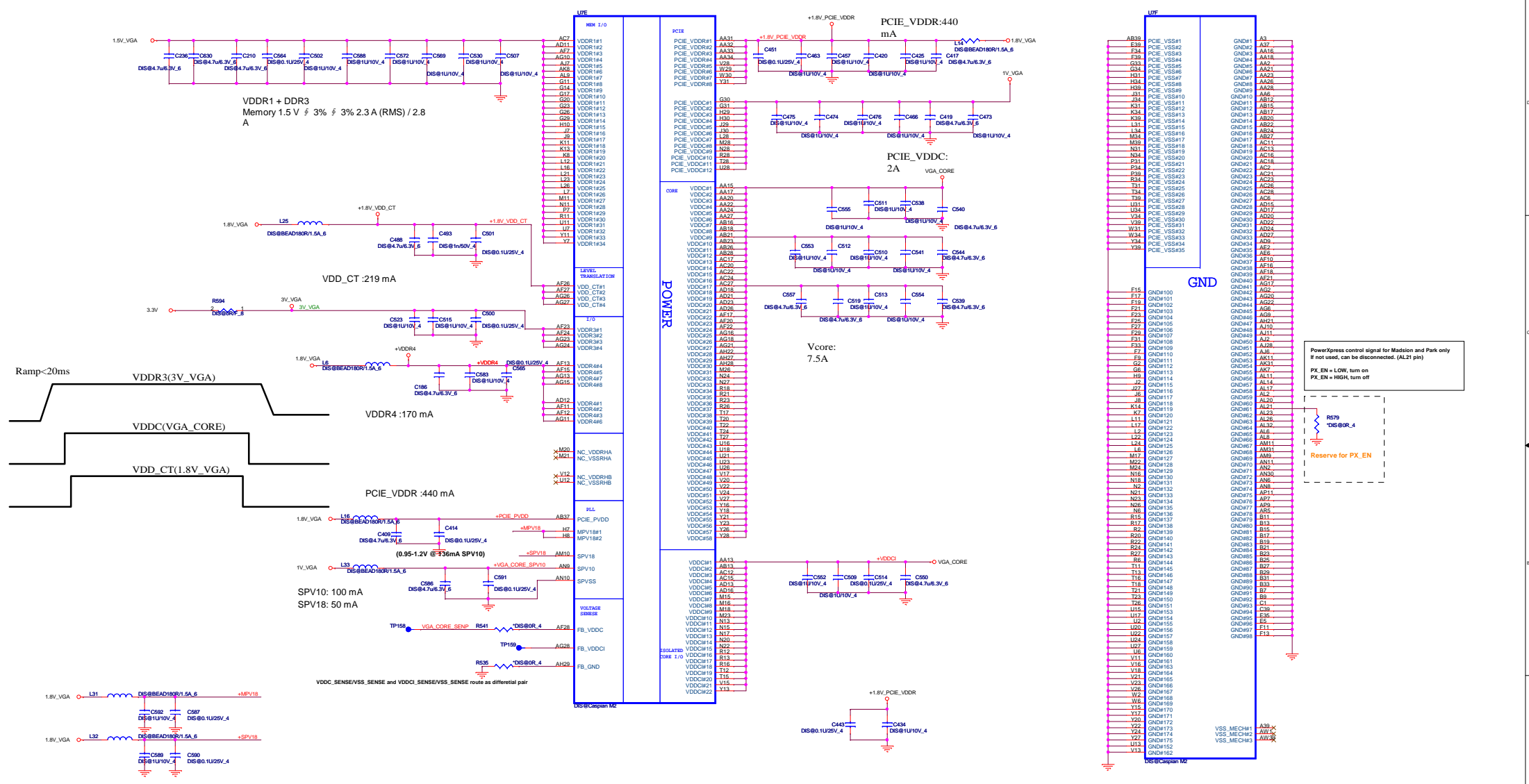
Fixed V _{DD}	1.0V
GFX_CORE_CNTRL0	H
GFX_CORE_CNTRL1	H



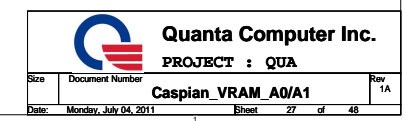
CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	Name	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing, Default setting for Desktop	
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	
BF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on. Note: 5.0 GT/s capability will be controlled by software.	
BF_VGA_DIS	GPIO9	VGA Disable determines whether or not the card will be recognized as the system's VGA controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	
BIOS_ROM_EN	GPIO22	ENABLE EXTERNAL BIOS ROM	1:enable 0:disable
ROMIDCFG2(0)	GPIO[13:11]	Primary Memory Aperture size requested Size of the primary memory apertures CONFID2[0] 128 MB 000 256 MB 001 512 MB 010 1 GB 011 Not Supported 100 Note:For frame buffers larger than 256 MB (e.g. 512 MB, 1 GB) the aperture size should be 256 MB.	
VIP_DEVICE_STRAP_ENA	DAC2_VSY	IGNORE VIP DEVICE STRAPS	1:enable 0:disable
AUDIO1[0] AUDIO[0]	EXT_CRT_HSYNC EXT_CRT_VSYNC	AUDIO1[0] AUDIO[0] 0 0 No audio function 1 0 Audio for DisplayPort and HDMI if idonfig is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	
RSVD RSVD	GPIO8 GPIO_21_BB_EN GENLK_CLK	Internal use only. Internal use only. Internal use only.	



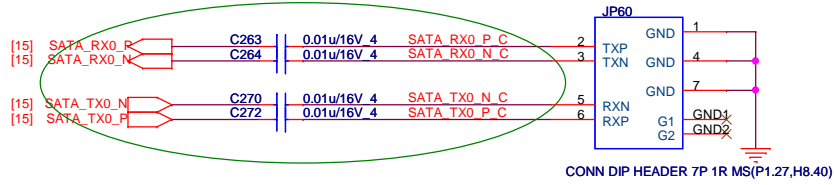




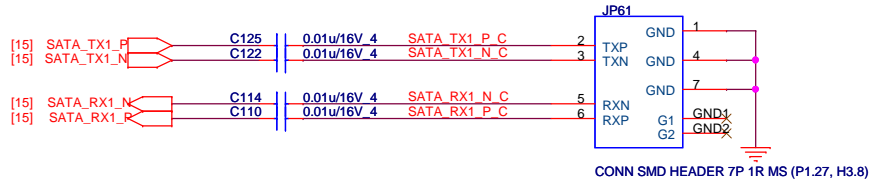
www.vinatix.vn



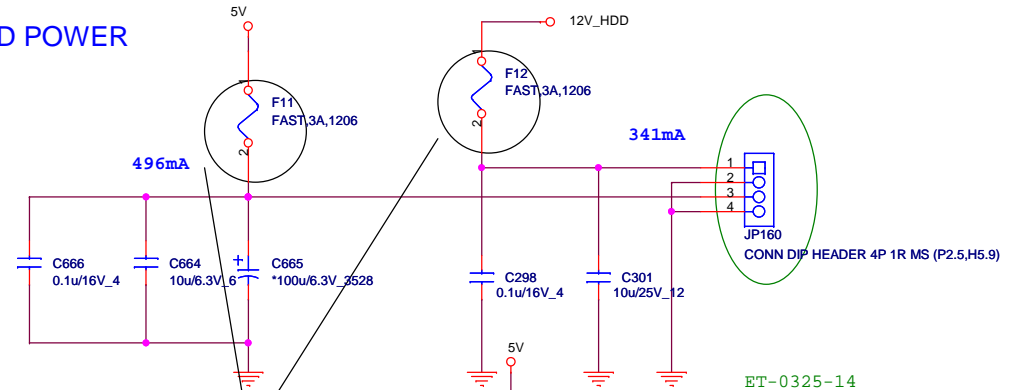
ET-0325-12



the same as QUX

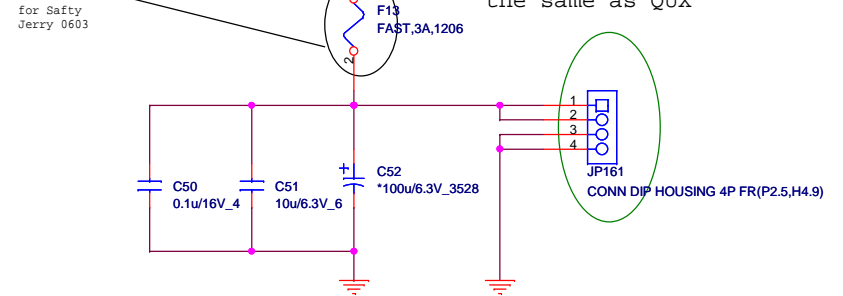


HDD POWER



ET-0325-14

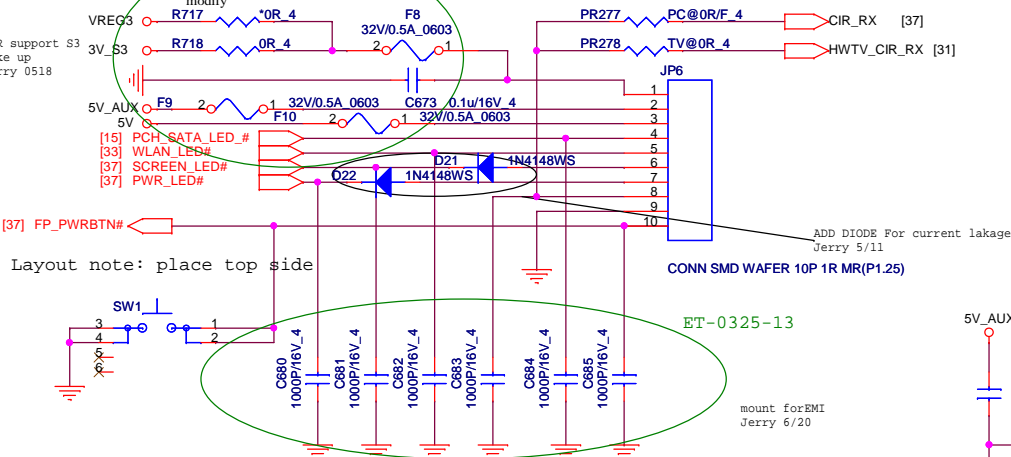
ODD POWER



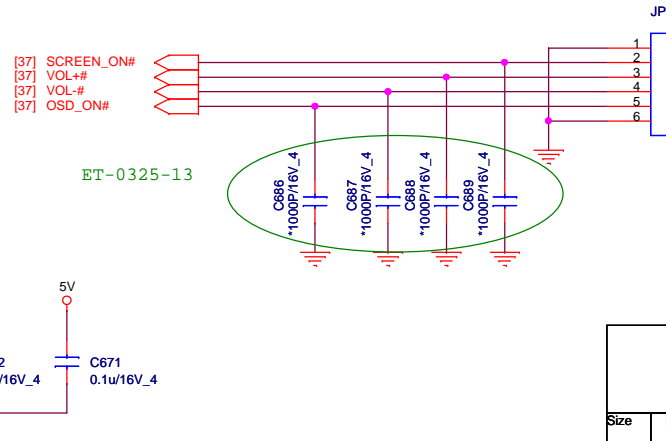
the same as QUX

Power Key

ET-0328-04
ET-0330-05



HotKey



Quanta Computer Inc.
PROJECT : QUA

Size	Document Number	Rev
	SATA HDD/ODD/Key	1A
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UMA

[36]	TMDSSB_DATA2+_LVS	R393	UMA@0R_4	HDMI_DATA2+		
[37]	TMDSSB_DATA2+_LVS	R394	UMA@0R_4	HDMI_DATA2+		
[38]	TMDSSB_DATA1+_LVS	R397	UMA@0R_4	HDMI_DATA1+		
[39]	TMDSSB_DATA1+_LVS	R398	UMA@0R_4	HDMI_DATA1+		
[40]	TMDSSB_DATA0+_LVS	R392	UMA@0R_4	HDMI_DATA0+		
[41]	TMDSSB_DATA0+_LVS	R391	UMA@0R_4	HDMI_DATA0+		
[42]	TMDSSB_CLK+_LVS	R396	UMA@0R_4	HDMI_CLK+		
[43]	TMDSSB_CLK+_LVS	R396	UMA@0R_4	HDMI_CLK+		

DIS

[23]	VGA_TMDSSB_DATA2+	R414	DIS@0R_4	HDMI_DATA2+		
[23]	VGA_TMDSSB_DATA2+	R415	DIS@0R_4	HDMI_DATA2+		
[23]	VGA_TMDSSB_DATA1+	R419	DIS@0R_4	HDMI_DATA1+		
[23]	VGA_TMDSSB_DATA1+	R419	DIS@0R_4	HDMI_DATA1+		
[23]	VGA_TMDSSB_DATA0+	R412	DIS@0R_4	HDMI_DATA0+		
[23]	VGA_TMDSSB_DATA0+	R413	DIS@0R_4	HDMI_DATA0+		
[23]	VGA_TMDSSB_CLK+	R416	DIS@0R_4	HDMI_CLK+		
[23]	VGA_TMDSSB_CLK+	R417	DIS@0R_4	HDMI_CLK+		

UMA

[36]	SDVO_CLK_TMDSSB_LVS	R381	UMA@0R_4	HDMI_SDVO_CLK		
[37]	SDVO_DAT_TMDSSB_LVS	R377	UMA@0R_4	HDMI_SDVO_DAT		

DIS

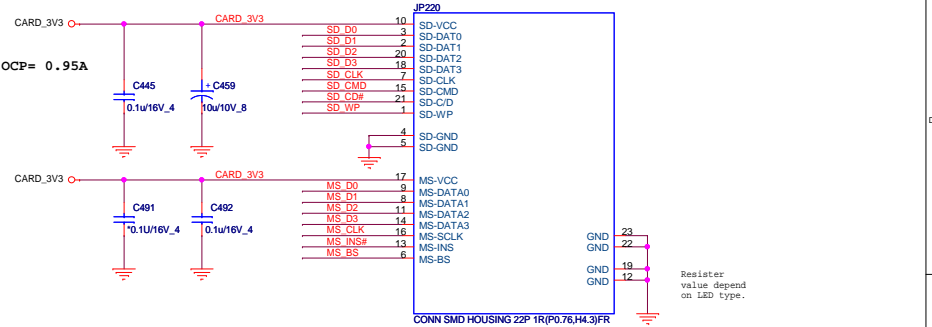
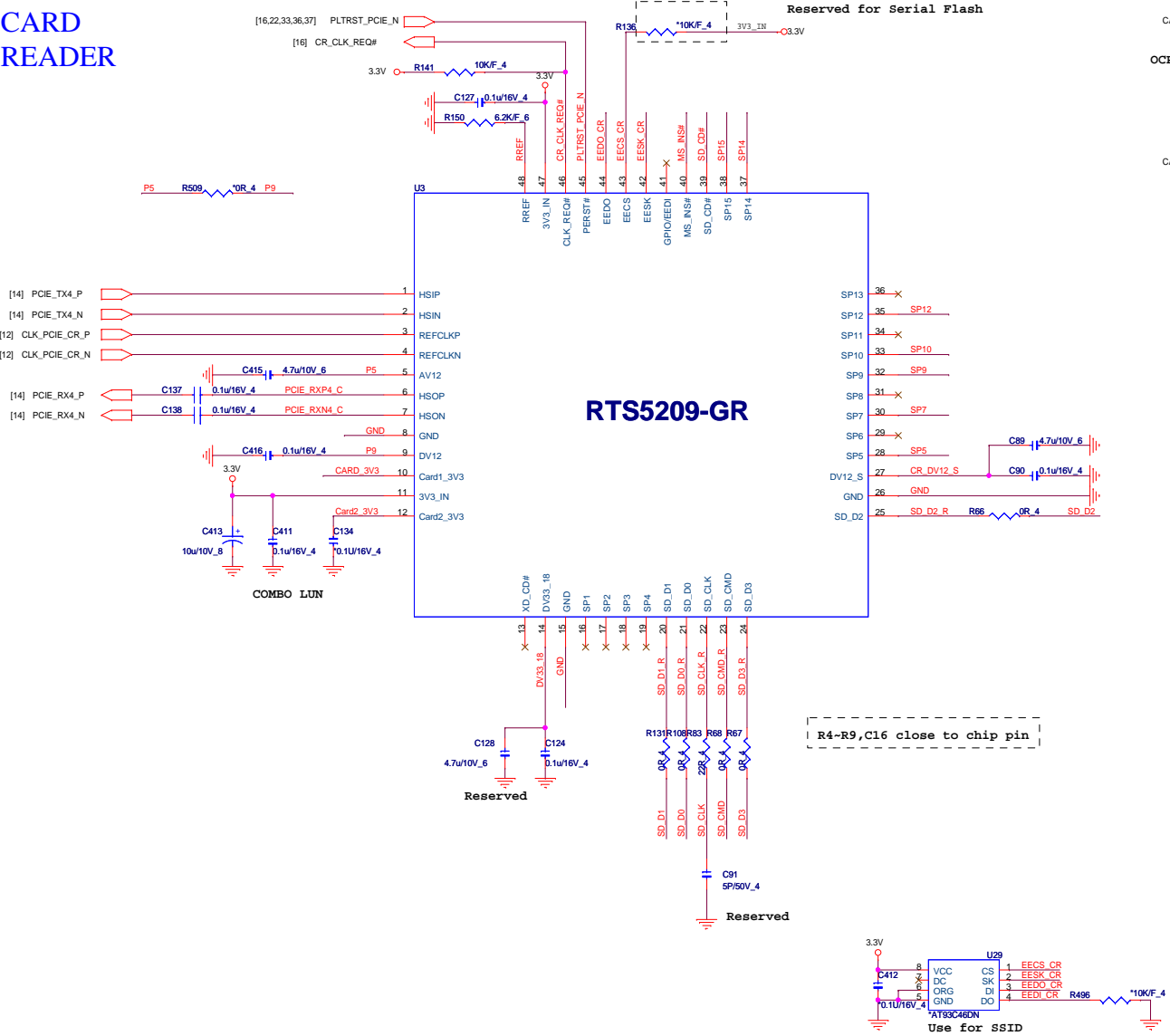
[23]	VGA_TMDSSB_DDC_CLK	R382	DIS@0R_4	HDMI_SDVO_CLK		
[23]	VGA_TMDSSB_DDC_CLK	R378	DIS@0R_4	HDMI_SDVO_DAT		

HDMI

[33]	HDMI_DATA2+		HDMI@0R_4		
[33]	HDMI_DATA2+		HDMI@0R_4		
[33]	HDMI_DATA1+		HDMI@0R_4		
[33]	HDMI_DATA1+		HDMI@0R_4		
[33]	HDMI_DATA0+		HDMI@0R_4		
[33]	HDMI_DATA0+		HDMI@0R_4		
[33]	HDMI_CLK+		HDMI@0R_4		
[33]	HDMI_CLK+		HDMI@0R_4		

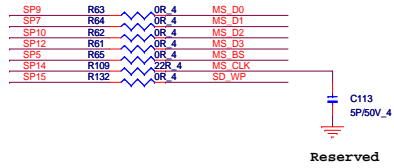
[illegible][illegible][illegible][illegible]


3 IN 1
CARD
READER



Share Pin

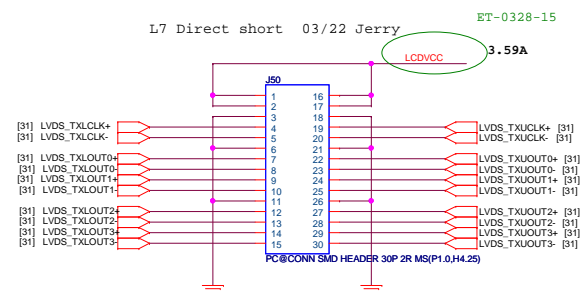
Share Pin	MS	SD
SP1		
SP2		
SP3		
SP4		
SP5	MS_BS	
SP6		
SP7	MS_D1	
SP8		
SP9	MS_D0	
SP10	MS_D2	
SP11		
SP12	MS_D3	
SP13		
SP14	MS_CLK	
SP15		SD_WP



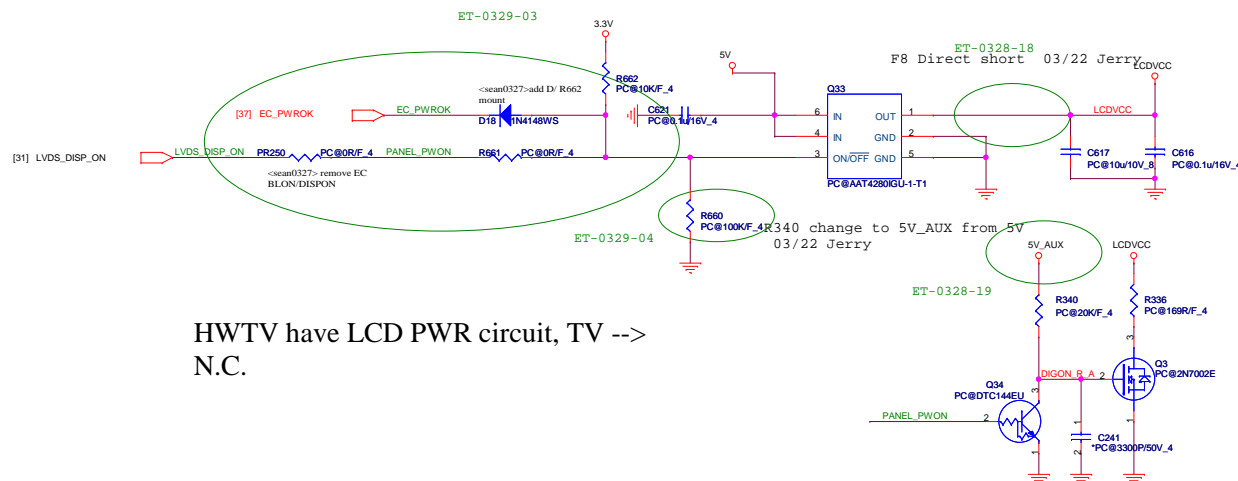
**Quanta Computer Inc.**
PROJECT : QUA

Size	Document Number	Rev
	Card Reader RTSS5209	1A
Date:	Monday, July 04, 2011	Sheet 32 of 48

LCD CONNECTOR

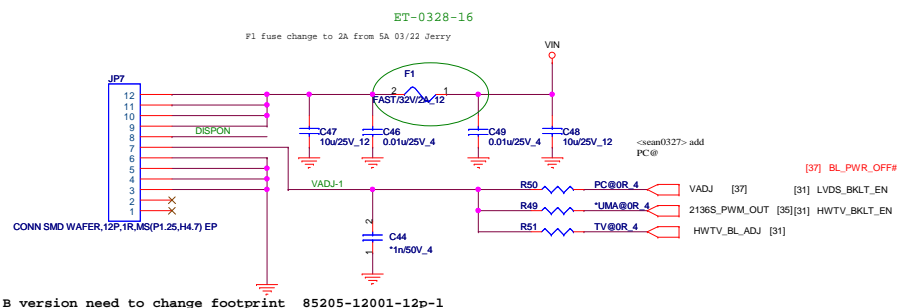


LCD POWER SWITCH

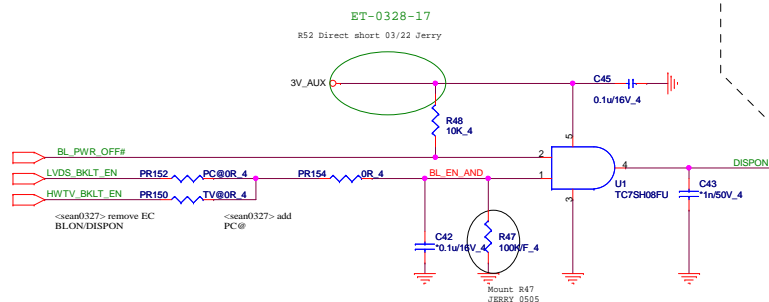


HWTV have LCD PWR circuit, TV --> N.C.

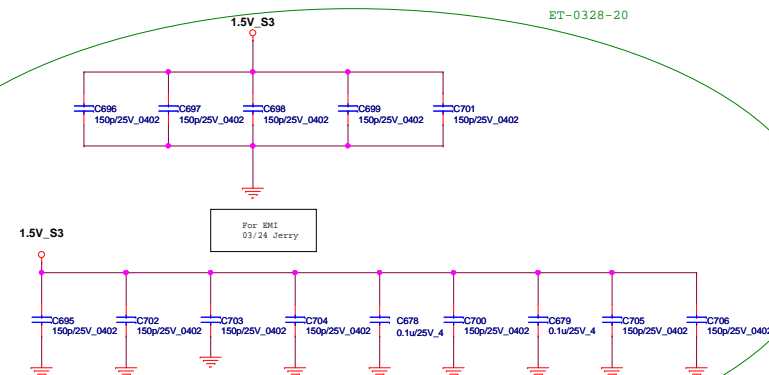
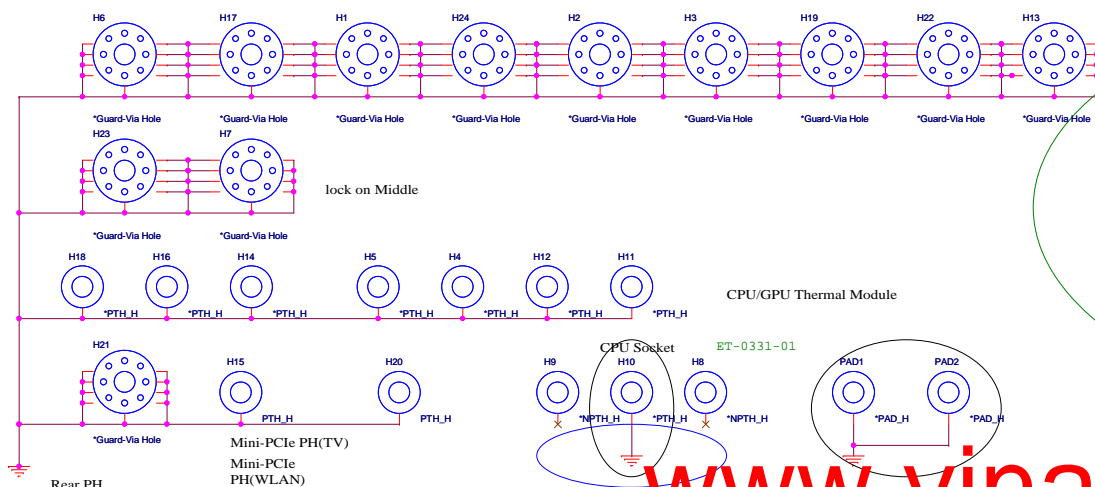
Converter B/D



BACKLIGHT CONTROL



Hole

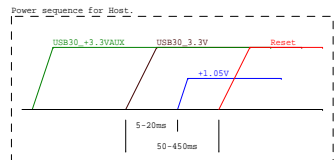


Schematic diagram of the SPI Flash ROM connection. The diagram shows four OVCUR pins (OVCUR1, OVCUR2, OVCUR3, OVCUR4) connected to resistors R187, R186, R185, and R184 respectively. These resistors are connected to the USB30 +3.3VAUX supply. The other end of the resistors is connected to the SPI Flash ROM chip (U31) at pins 1 (SPICSS), 2 (SPICL6), 3 (SPICL5), 4 (SPICL4), 5 (SI), 6 (SO), 7 (HOLD1), 8 (VDD), 9 (VSS), and 10 (WPH). The chip is labeled 'W39M02512MC-12G'.

[illegible][illegible]

U5	66	VDD	VSUS33
	67	VDD	VSUS33
	68	VDD	VSUS33
	69	YSRIS3	USBHFE2#
	70	YSRIS3	USBHFE3#
	71	SMAT	USBHFE4#
	72	PEXMT1	SPISO
	73	PEXMT2	SPISCS
	74	PEWAKE	SPBCLK
	75	75, 77, 77	SPIVSS
	76	LPTVREN	VSUS33
	77	VSUS33	VSUS33
	78	VSUS33	VSUS33
	79	GND	JTAGCK
	80	VSUS33	VSUS33
	81	VSUS33	VSUS33
	82	VSUS33	VSUS33
	83	VSUS33	VSUS33
	84	VSUS33	VSUS33
	85	VSUS33	VSUS33
	86	VSUS33	VSUS33
	87	VSUS33	VSUS33
	88	VSUS33	VSUS33
	89	VSUS33	VSUS33
	90	VSUS33	VSUS33
	91	VSUS33	VSUS33
	92	VSUS33	VSUS33
	93	VSUS33	VSUS33
	94	VSUS33	VSUS33
	95	VSUS33	VSUS33
	96	VSUS33	VSUS33
	97	VSUS33	VSUS33
	98	VSUS33	VSUS33
	99	VSUS33	VSUS33
	100	VSUS33	VSUS33
	101	VSUS33	VSUS33
	102	VSUS33	VSUS33
	103	VSUS33	VSUS33
	104	VSUS33	VSUS33
	105	VSUS33	VSUS33
	106	VSUS33	VSUS33
	107	VSUS33	VSUS33
	108	VSUS33	VSUS33
	109	VSUS33	VSUS33
	110	VSUS33	VSUS33
	111	VSUS33	VSUS33
	112	VSUS33	VSUS33
	113	VSUS33	VSUS33
	114	VSUS33	VSUS33
	115	VSUS33	VSUS33
	116	VSUS33	VSUS33
	117	VSUS33	VSUS33
	118	VSUS33	VSUS33
	119	VSUS33	VSUS33
	120	VSUS33	VSUS33
	121	VSUS33	VSUS33
	122	VSUS33	VSUS33
	123	VSUS33	VSUS33
	124	VSUS33	VSUS33
	125	VSUS33	VSUS33
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	129	VSUS33	VSUS33
	130	VSUS33	VSUS33
	131	VSUS33	VSUS33
	132	VSUS33	VSUS33
	133	VSUS33	VSUS33
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	155	VSUS33	VSUS33
	156	VSUS33	VSUS33
	157	VSUS33	VSUS33
	158	VSUS33	VSUS33
	159	VSUS33	VSUS33
	160	VSUS33	VSUS33
	161	VSUS33	VSUS33
	162	VSUS33	VSUS33
	163	VSUS33	VSUS33
	164	VSUS33	VSUS33
	165	VSUS33	VSUS33
	166	VSUS33	VSUS33
	167	VSUS33	VSUS33
	168	VSUS33	VSUS33
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	172	VSUS33	VSUS33
	173	VSUS33	VSUS33
	174	VSUS33	VSUS33
	175	VSUS33	VSUS33
	176	VSUS33	VSUS33
	177	VSUS33	VSUS33
	178	VSUS33	VSUS33
	179	VSUS33	VSUS33
	180	VSUS33	VS

The diagram illustrates the wiring for a USB Down Port. It shows several power lines: 3V_S3 (purple), 3.3V (purple), 1.05V (cyan), 5V_S3 (pink), USB30_+3.3VAUX (orange), USB30_3.3V (brown), USB30_1VE (cyan), USB30_1VL (cyan), and USB30_5V_S3 (pink). The connections are as follows: 3V_S3 is connected to USB30_+3.3VAUX. 3.3V is connected to USB30_3.3V. 1.05V is connected to USB30_1VE and USB30_1VL. 5V_S3 is connected to USB30_5V_S3. A note in a box states: "For USB Down Port USB30_5V_S3".



X'tal 25MHz

[12] CLKOUT_25M

R164

'USB3@0R/F 6

C149

USB@33P/50V 4

R161

USB3@0R/F 6

SSXI

Y1

USB3@25MHz/30PPM

C141

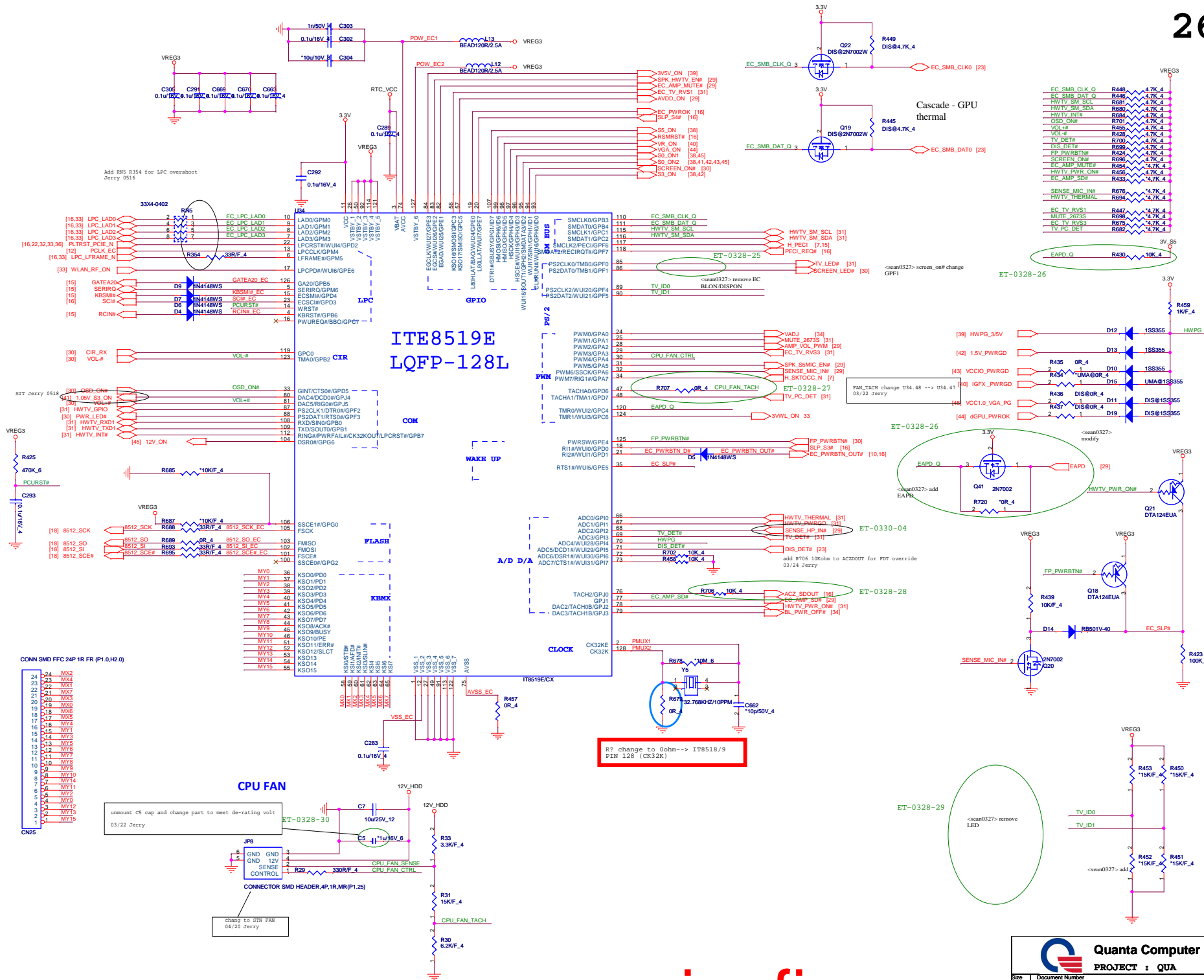
USB@33P/50V 4

SSXO

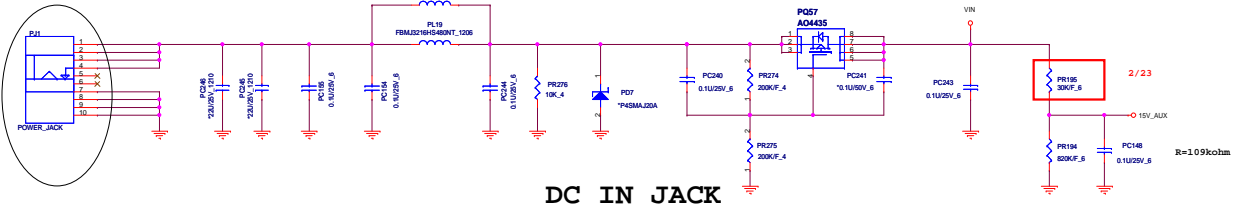
BG625000737/B/G6250004086

XTL-5_3X3_2-1_8-1

Crystal foot print must be reserved in case 25MHz clock from clock generator is not stable enough.

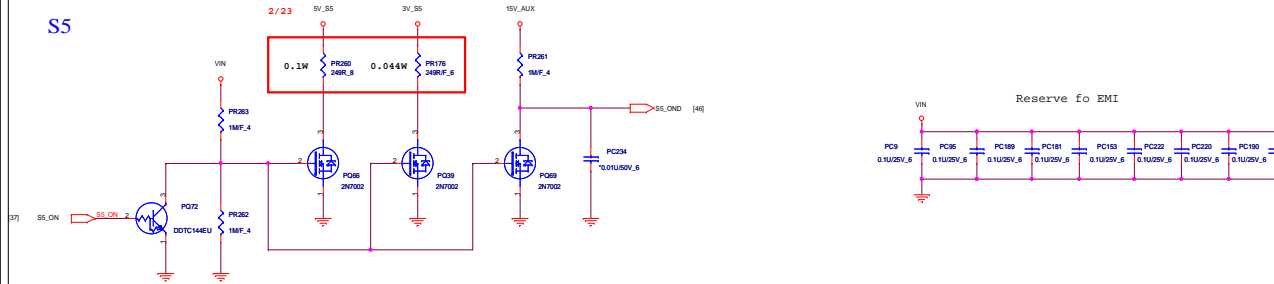


```
ramp-up time for all power rails
50 us <All power rails except 5V_S5 <40 ms
100 us <5V_S5<40 ms
```

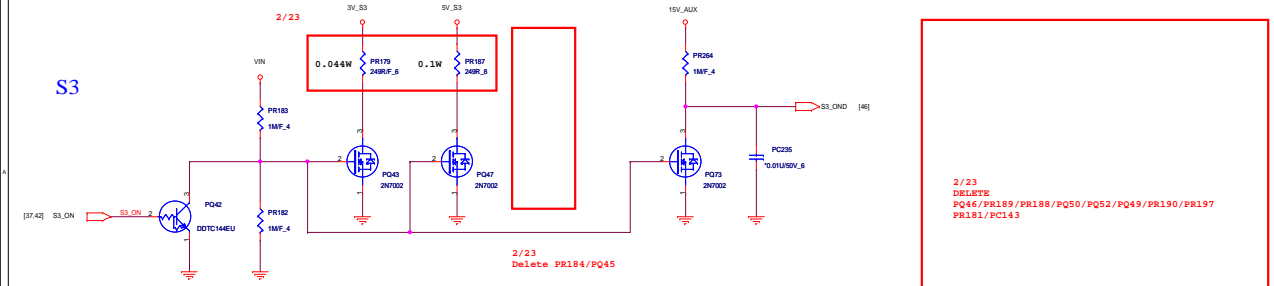


DC IN JACK

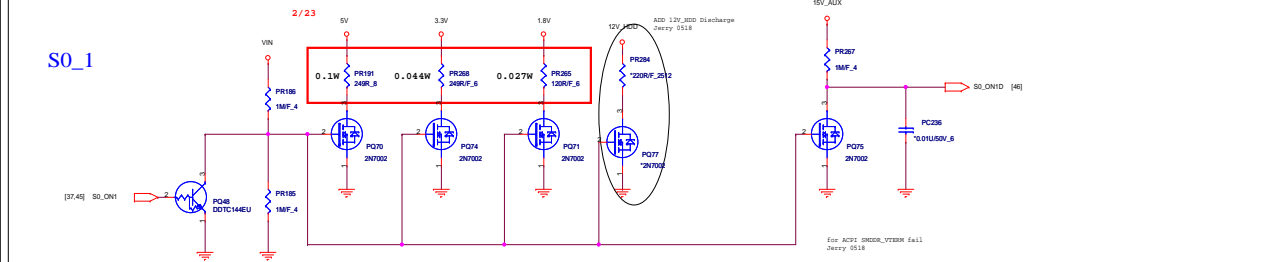
S5



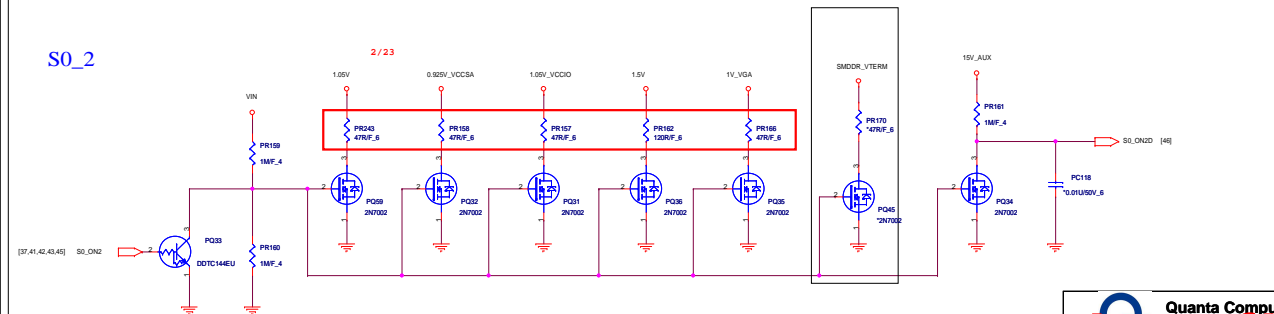
S3



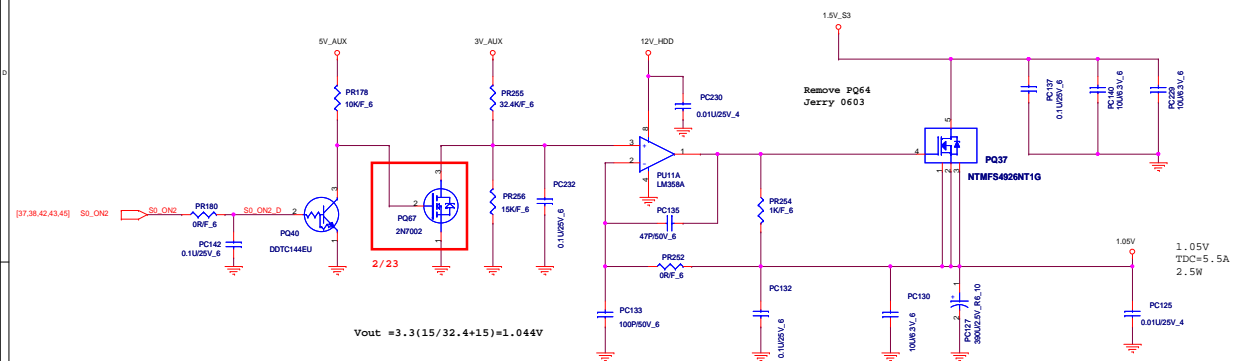
S0_1



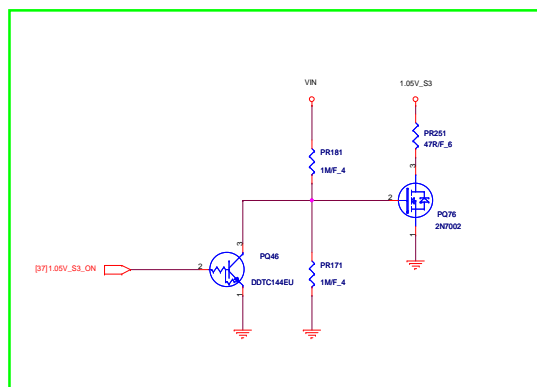
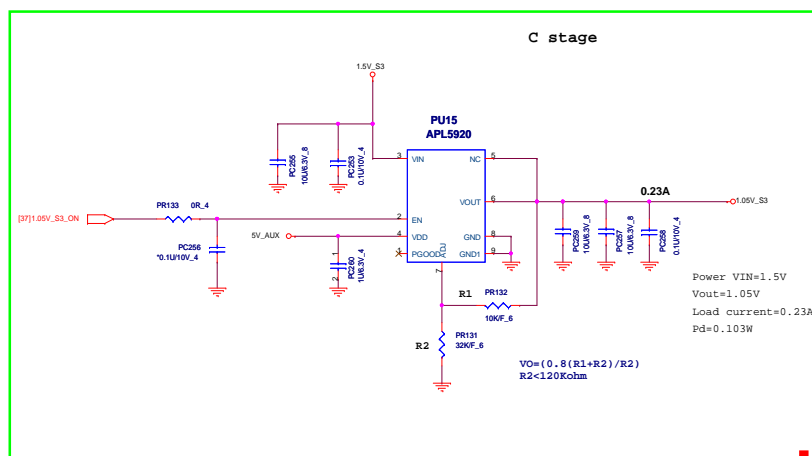
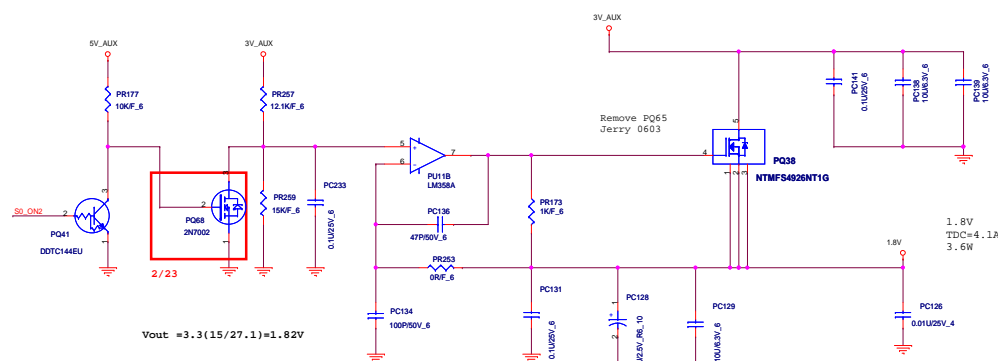
S0_2

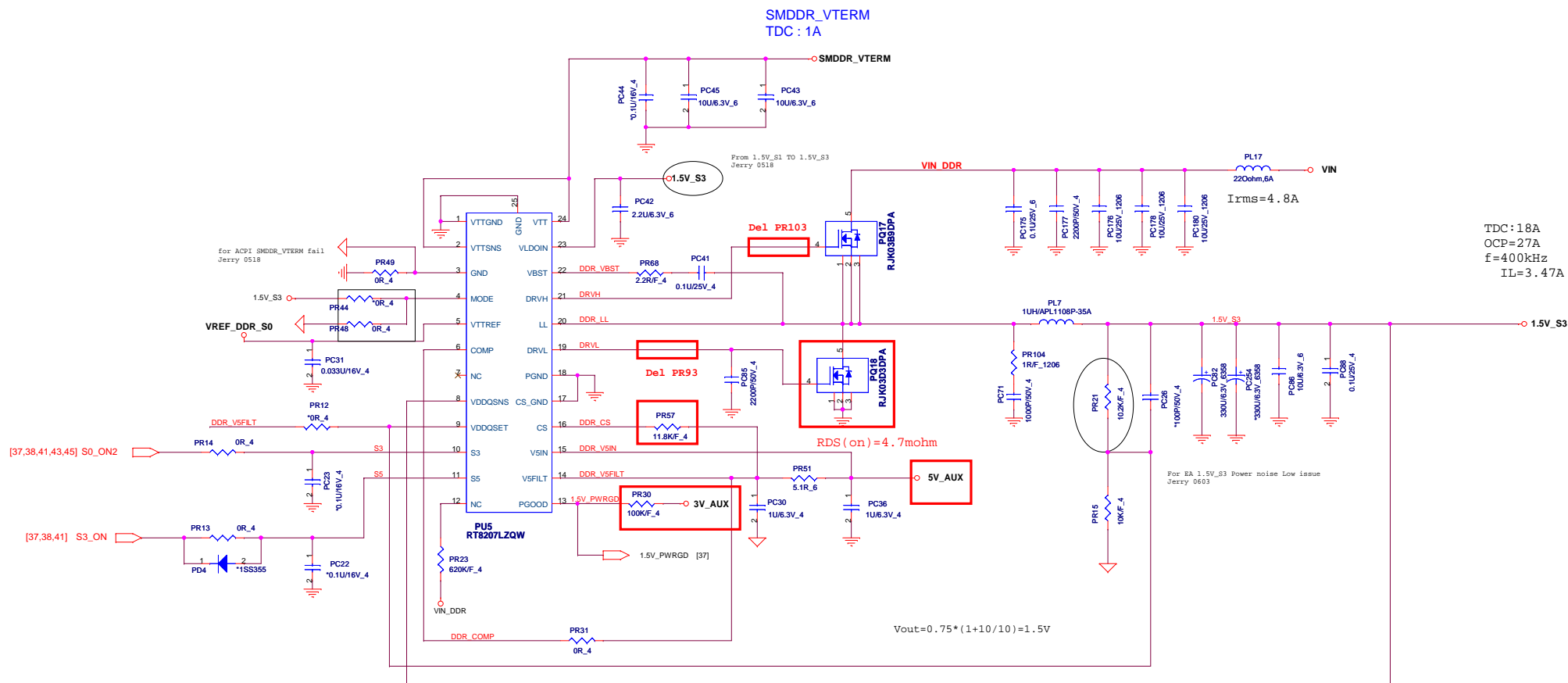


VCC1.05 FOR PCH



VCCPLL





ESR=7mohm
V=3.47*7=24.3mV

$R(I_{lim}) = (I_{lim}(27A) - 3.47A/2) * 4.7(ohm)/10u$
=11.86K (ohm) ---->11.8K (ohm) (PR57)



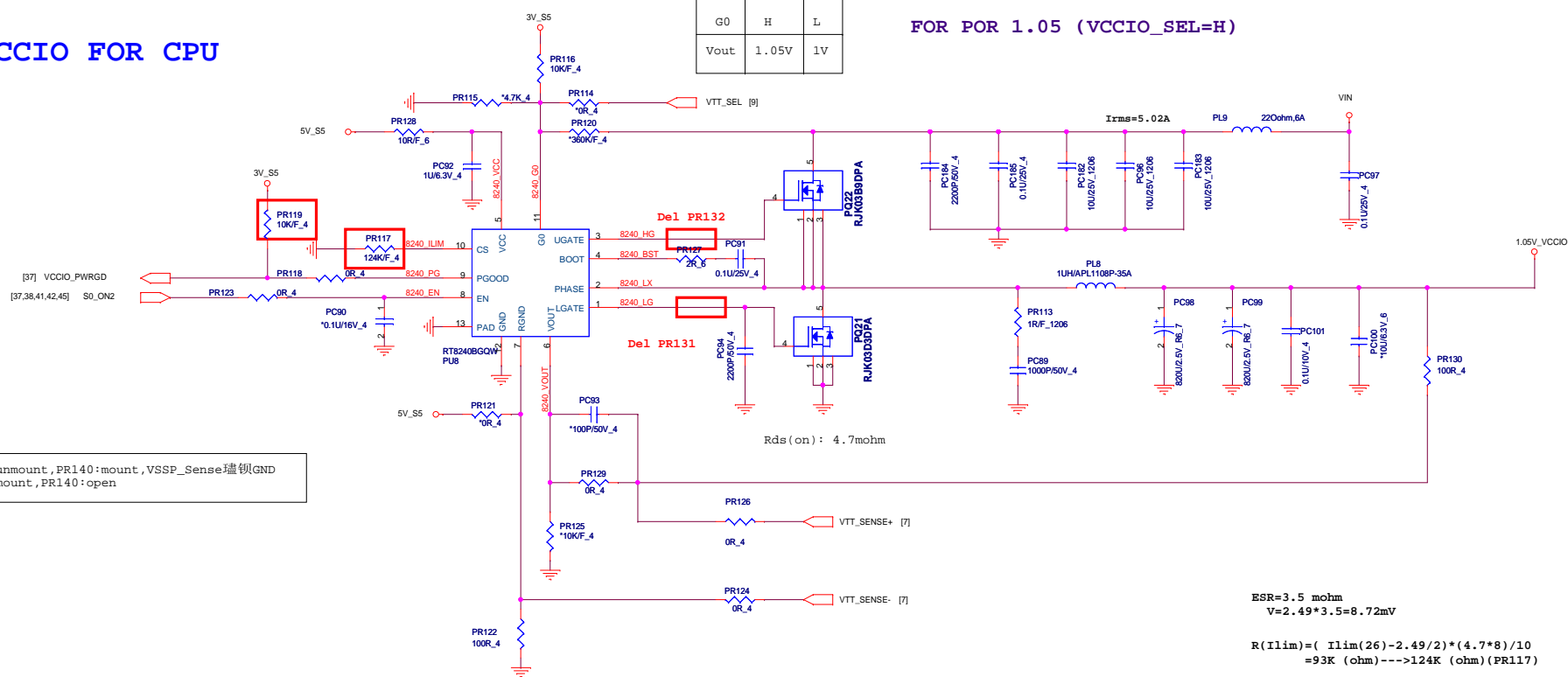
Quanta Computer Inc.
PROJECT : QUA

Size	Document Number	Rev
	1.5VSUS(RT8207A)SMDDR_VTERM	1A
Date:	Monday, July 04, 2011	Sheet 42 of 48

VCCIO FOR CPU

G0	H	L
Vout	1.05V	1V

FOR POR 1.05 (VCCIO_SEL=H)



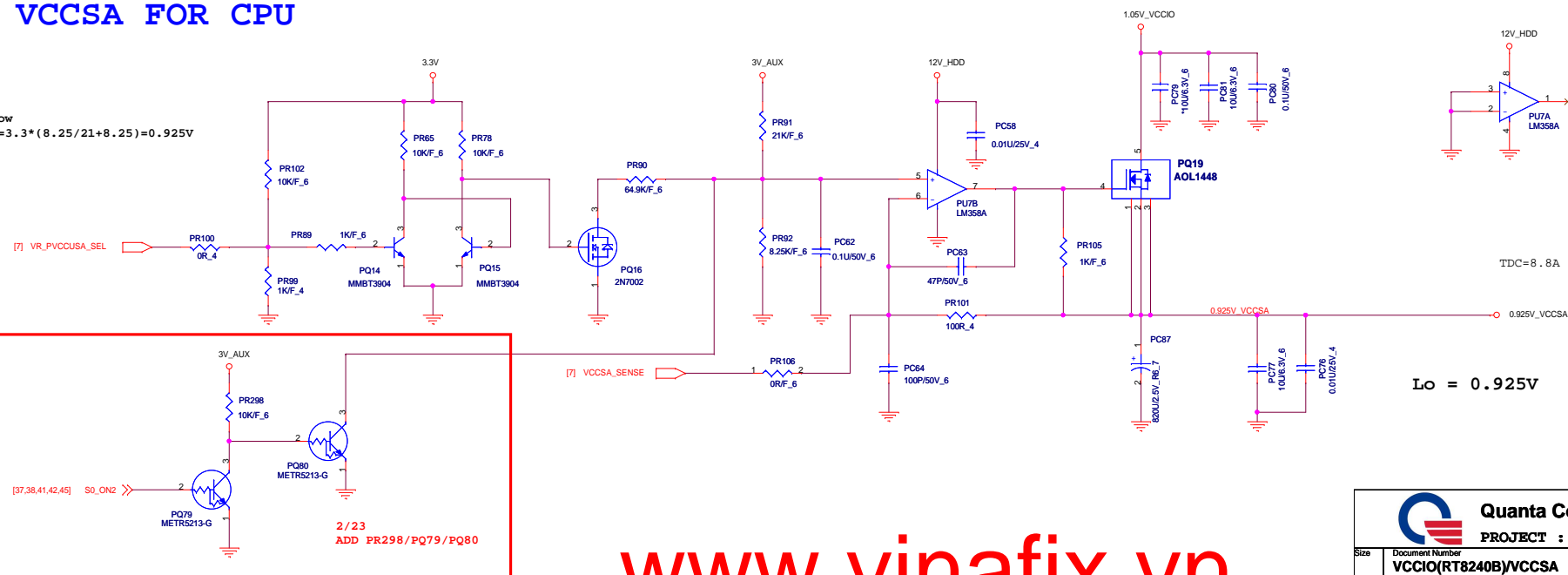
Fix $V_{out}=1.05V$

TDC=17.4A
f=400KHz
IL=2.49A
OCP=26A

```
CPU:unmount,PR140:mount,VSSP_Sense端钨GND
CPU:mount,PR140:open
```

VCCSA FOR CPU

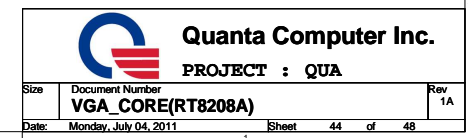
EN: Low
 $V_{out} = 3.3 * (8.25 / 21 + 8.25) = 0.925V$



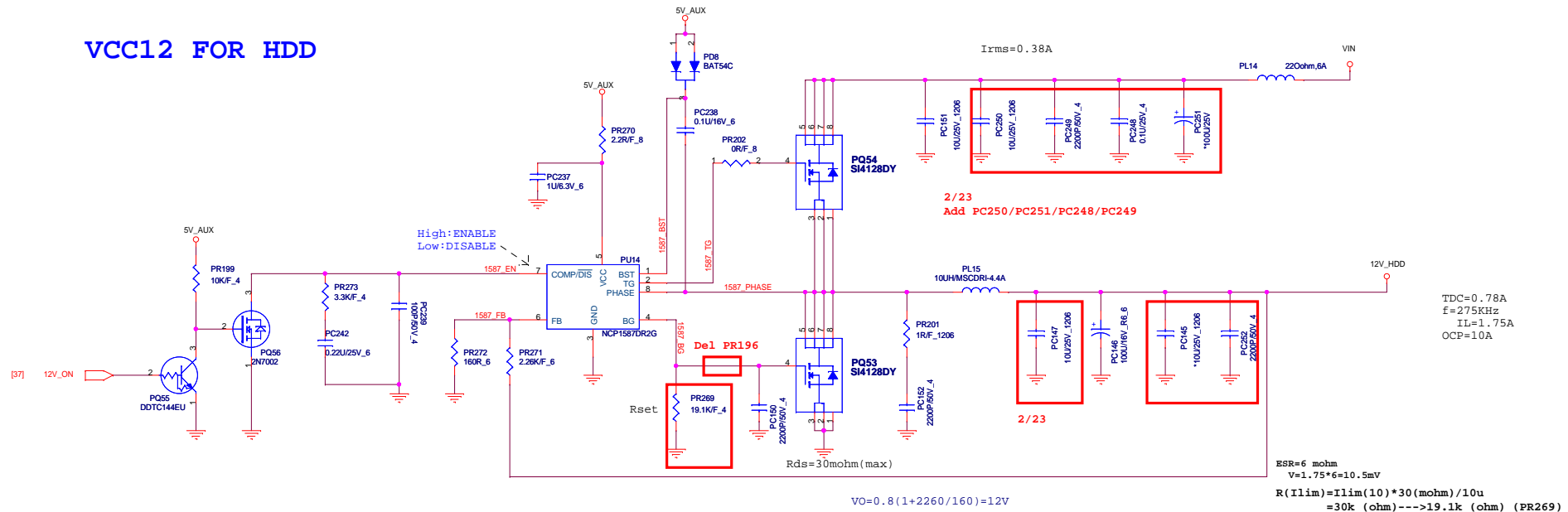
TDC=8.8A

$$L_O = 0.925V$$

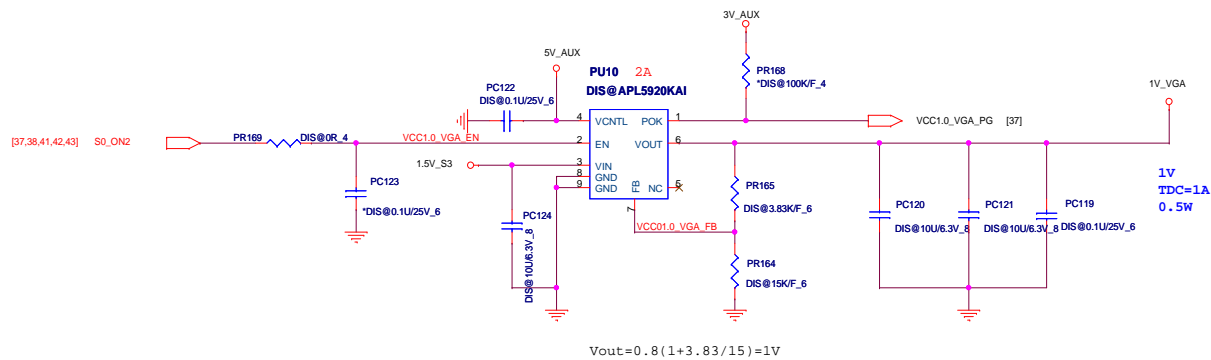
www.vinafix.vn



VCC12 FOR HDD

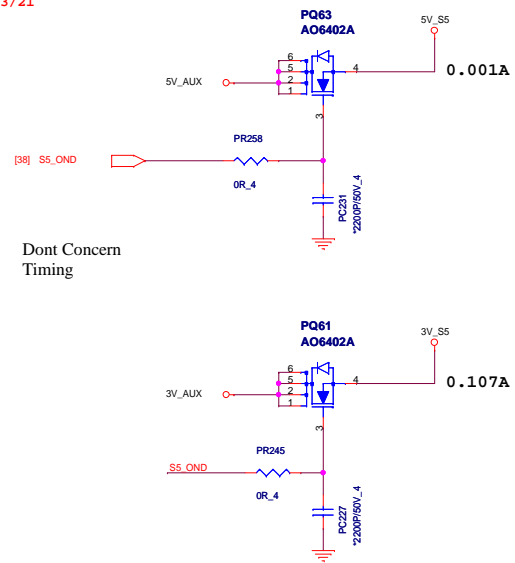


VCC1.0_VGA

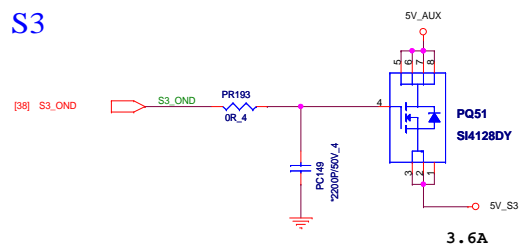


S5

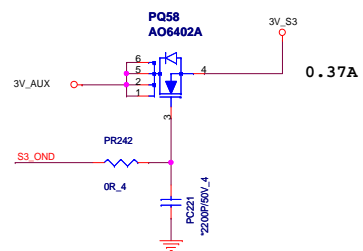
3/21



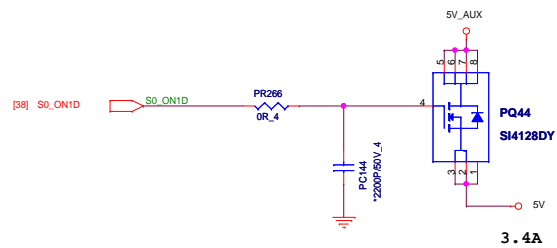
S3



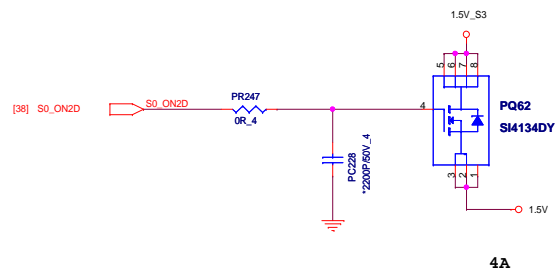
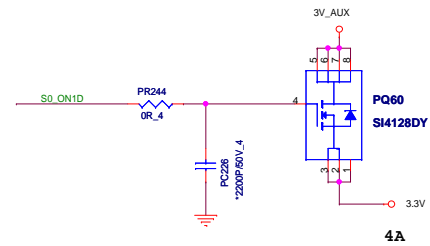
Dont Concern Timing



S0



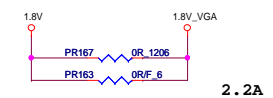
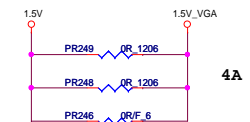
Dont Concern Timing



AMP/TV



VGA



Quanta Computer Inc.

PROJECT : QUA

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	LOAD SWITCH	1A
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ET Change List

Item	Page	Reason	Detail
ET-0325-01	15	SATA3GP Pull up 10kohm for reserve	Add R704 for reserve
ET-0325-02	16	SCI# change to GPIOL2 request from BIOS	GPIOS3 change to GPIOL2 for SCI#
ET-0325-03	23	AUD0, AUD1 strap pin pull high for HDMI display	Stuff R133, R134 10Kohm
ET-0325-04	23	VGA_TMDSB_HOT_PLUG short to 3V_VGA	Remove 3V_VGA on VGA_TMDSB_HOT_PLUG
ET-0325-05	23	Add 0ohm for VGA_TMDSA_DDC_CLK & VGA_TMDSA_DDC_CLK	R710, R711 for reserve
ET-0325-06	28	Change footprint for SMT issue	J71 footprint to usb-020173gr004e417z1-4p-r
ET-0325-07	28	Add HCB1608KF-471T10/0.2ohm * 2 22P/50V_4 * 2 for EMI	Add L36, L38, C693, C694
ET-0325-08	28	F6 change to 0.5 A from 1.1A for Camera fit	F6 change to 0.5A from 1.1A
ET-0325-09	28	C294 change to 330uF from 470uF	C294 change to 330uF from 470uF
ET-0325-10	28	Add 4.7uF for touch moudle	Add C674 4.7uF
ET-0325-11	29	Add 1k for limit large current when Q9 turn on	Add R54 1Kohm
ET-0325-12	30	SATA TX & RX swap for SATA connector reverse	SATA_RX0_P_C, SATA_RX0_N_C, SATA_TX0_N_CSATA_TX0_P_C SWAP
ET-0325-13	30	Add 10pcs 1000pf for Power & Hotkey signal by EMI request	Add C680, C681, C682, C683, C684, C685, C686, C687, C688, C689
ET-0325-14	30	Correct JP160, JP161 footprint	JP160 --> 20288-04413-4p-1 J161 --> 20288-04413-4p-1
ET-0325-15	31	Add 0ohm 3pcs & 3pcs 10pf for EMI	Add R581, R708, R709 0ohm, C675, C676, C677 10pF
ET-0325-16	08	change CPU_CORE cap. to 22uF from 10uF & 330uF for CPU transiting issue	C14, C17, C19, C23, C26, C27, C29, C30, C31, C32, C335, C340, C345, C349, C354, C355, C360, C361, C690, C691, C692 change to 22uF from 10uF Add C707 330uF
ET-0328-01	31	Add R713 10Kohm & Q39 2N7002 for SATA LED	Add R713 10kohm & Q39 2N7002
ET-0328-02	23	R562 Change footprint to RC0402 from short0402	R562 Change footprint in BOM
ET-0328-03	24	Reference name error	C598 & C603 5.11kohm change to R715 & R716 5.11ohm
ET-0328-04	30	Power S/W connector add Fuse 0.5A for safety	Add R717, R718 0ohm stuff R717 for PC Add F8, F9, F10 0.5A for Fuse Add C673 0.1uF
ET-0328-05	31	Add 3pcs 0ohm & 3pcs 10pf for HW_TV_CRT for EMI	Add R581, R708, R709 0ohm Add C675, C676, C677 10pF
ET-0328-06	31	Add 4.7kohm for VGA_LVDS_CLK & VGA_LVDS_DAT pull up	Add R431, R432 4.7kohm
ET-0328-07	33	Add R623 10Kohm & Q40 DTC144EU for WLAN_LED	Add R623 10kohm & Q40 DTC144EU
ET-0328-08	33	Change D15 to R712 0ohm for CE control	Chagne D15 to R712 0ohm
ET-0328-09	33	Delete L36, don't need diode	Del L36
ET-0328-10	33	R403 change to 0603 from 0402 for margin	R403 change to 0603 0ohm
ET-0328-11	33	R360 change to 200kohm follow AMD recommend	R360 change to 200kohm from 10kohm
ET-0328-12	33	VGA_TMDSB_HOT_PLUG form Q7.3 to Q7.1 for correct connect	VGA_TMDSB_HOT_PLUG form Q7.3 to Q7.1
ET-0328-13	33	USBPWR_45, USBPWR_23 divide voltage to 3.3v from 2.5v	R364, R365 change to 10kohm from 33Kohm R353, R354 change to 15Kohm from 30kohm
ET-0328-14	33	F2, F3 change to Poly fuse 1.5A from fast fuse 5A for fit	F2, F3 change to Poly fuse 1.5A from 5A
ET-0328-15	34	Delete L7, don't need	Del L7
ET-0328-16	34	F1 change to 2A from 5A for fit	F1 change to 2A from 5A
ET-0328-17	34	Delete R52 0ohm direct short	Del R52
ET-0328-18	34	Delete F8 fuse direct short	Del F8
ET-0328-19	34	R340 pin1 change to 5V_AUX from 5V for discharge	R340 pin1 change to 5V_AUX from 5V for discharge
ET-0328-20	34	Add 150pf 12pcs & 0.1uf 2pcs for 1.5V_S3 by EMI request	Add C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706 for 150pF Add C678, C679 for 0.1uF
ET-0328-21	36	Stuff R207, R211 for PCH USB interface No stuff R615, R627 for cancel from VL801	Stuff R207, R211 0ohm, No stuff R615, R627
ET-0328-22	36	J70 change footprint for SMT issue	J70 change to usb-ueall1uc-r14u3-7h-9p
ET-0328-23	36	USB0_PWR divide voltage to 3.3v from 2.5v	R656 change to 10kohm from 33kohm R654 change to 15kohm from 30kohm
ET-0328-24	36	C141, C149 change to 33pF from 18pF to meet spec	C141, C149 change to 33pF from 18pF
ET-0328-25	37	U34.85 change to TV_LED# remove EC_DISP_ON	U34.85 change to TV_LED#
ET-0328-25	37	SCREEN_LED# U34.16 change to U34.86 for LED light	SCREEN_LED# U34.16 change to U34.86 for LED light
ET-0328-26	37	Add Q41 2N7002 & R430 10Kohm for EAPD leakage issue	Add Q41 2N7002, R430 10kohm R720 10kohm for reserve
ET-0328-27	37	EC U34. 47(CPU_FAN_TACH) & 48 (TV_PC_DET)swap	Add R707 0ohm
ET-0328-28	37	add R706 10Kohm to ACZDOUT for FDT override	Add R706 10kohm damping resistor
ET-0328-29	37	don't need LED debug	Del R460, LED1, Q23
ET-0328-30	37	C5 2.2uF 10V Derating fail	C5 change to 1uF/16V from 2.2uF/10V
ET-0329-01	37	Add 0.1uF for ESD	Add C710 0.1uF
ET-0329-02	16	Add 0.1uF for ESD	Add C710 0.1uF
ET-0329-03	14	Add 0.1uF for ESD	Add C709 0.1uF
ET-0329-04	20	Add 0.1uF for ESD	Add C598 0.1uF
ET-0329-05	20	Add 0.1uF for ESD	Add C603 0.1uF
ET-0329-06	36	Add 330uF for USB drop	Add 330uF
ET-0329-07	36	Add R719 0ohm for PCIE_WAKE#	Add R719 0ohm
ET-0329-08	35	Change L8 footprint for SMT issue	Change L8 footprint to L3x3-1
ET-0329-09	07	Add 0ohm 7pcs for ESD	Add R52, R460, R259, R705, R721, R722, R723 0oh

ET Change List for Power

A stage TO B stage Upate

- 1.Change PR260/PR176/PR179/PR187/PR191/PR268/PR265/PR243/PR158/PR157/PR162/PR166 for discharge resistor spec.
- 2. DELETE PQ46/PR189/PR188/PQ50/PQ52/PQ49/PR190/PR197/ PR181/PC143 (3V/5V_AUX discharge)
- 3. Delete PR184/PQ45 for 1.5V_S3 discharge
- 4. Mount PC187 for 5V_AUX ripple
- 5. Mount PC218 for 3V_AUX ripple
- 6. Change PQ27(SI4812 to SI4134)/PR227(309Kohm to 267Kohm) for 5V_AUX OCP
- 7. Change PQ29(SI4812 to SI4134)/PR232(357Kohm to 294Kohm) for 3V_AUX OCP
- 8. Change PR147(1 ohm to 1.5 ohm)/PC107(1000pF to 1500pF) to reduce 5V_AUX spike voltage
- 9. Change PC61(3300pF to 2200pF) /PC68 (100pF to 330pF) for Vcore compensation
- 10.Change PR83(32.4kohm to 23.2Kohm) for Vcore OCP
- 11.Change PR35 (16.2Kohm to 22.6kohm) for Vauxg loadline
- 12.Change PC143(1500pF to 330pF) for Vauxg RC match
- 13.Change PR38 (30.9kohm to 33.2Kohm) for Vauxg OCP
- 14.Change PR110(3.3kohm to 4.7Kohm) for Vcore DVID
- 15.Change PR117 (47kohm to 124Kohm)for VCCIO OCP
- 16.Add PR298/PQ79/PQ80 for VCCSA_0.925V on pin control
- 17.Unmount PR151/PC109/PC108 to increase VGA_Core efficiency
- 18.PR269 (30kohm to 19.1kohm) for 12V_HDD OCP
- 19.Add PC147/PC252 for EMI request
- 20.Change PQ58/PQ61/PQ63(SI4128 to AO6402A) for low switch cost down
- 21.Reserve PC253 100uFfor 12V_VDD MLCC noise
- 22.Reserve PC247 100uF for 3/5V MLCC noise
- 23.PR57(15kohm to 11.8kohm) for 1.5V_S3
- 24.Del PR230/PR239/PR240/PR225 for gate resistor
- 25.Del PR93/PR103 for gate resistor
- 26. 27.mount PR30
- 28.1.5V_S3,PG pin change to 3V_AUX
- 29.V5FILT change to 5V_AUX
- 30.DEL PR131/PR132 for gate resistor
- 31.mount PR119
- 32.mount PR119
- 33.Del PR148/PR153
- 34.Unmount PC116
- 35.mount PC250
- 36.Del PR169 for gate resistor